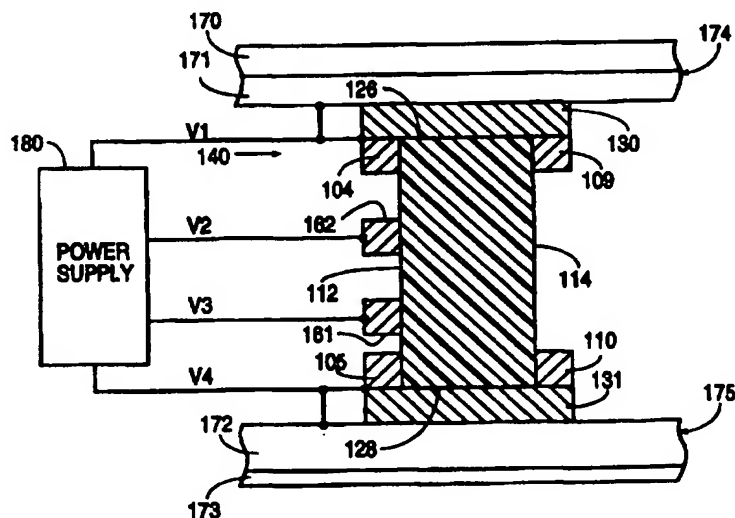




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(54) Title: SPACER STRUCTURES FOR USE IN FLAT PANEL DISPLAYS AND METHODS FOR FORMING SAME



(57) Abstract

The invention provides spacers for separating and supporting a faceplate structure and a backplate structure in a flat panel display, and methods for fabricating these spacers. Each spacer is typically made of ceramic, such as alumina, containing transition metal oxide, such as titania, chromia or iron oxide. Each spacer can be fabricated with an electrically insulating core and electrically resistive skins. The insulating core can be a wafer formed of ceramic such as alumina, and the resistive skins can be formed by laminating electrically resistive wafers, formed from alumina containing transition metal oxide, to the outside surfaces of the insulating core. Each spacer can also have a core of electrically insulating ceramic composition made of a ceramic containing a transition metal oxide in its higher oxide states, and electrically resistive outside surfaces made of a ceramic containing a transition metal oxide in lower oxide states. Face and/or edge metallization strips can optionally be provided on each spacer.

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SPACER STRUCTURES FOR USE IN FLAT PANEL DISPLAYS
AND METHODS FOR FORMING SAME

5 BACKGROUND OF THE INVENTION

1. Field of the Invention

 This invention relates to flat panel devices such
as a flat cathode ray tube (CRT) display. More
particularly, this invention relates to a spacer
10 structure for internally supporting a faceplate
structure and a backplate structure of a flat panel
device.

2. Related Art

15 Numerous attempts have been made in recent years
to construct a flat CRT display (also known as a "flat
panel display") to replace the conventional deflected-
beam CRT display in order to provide a lighter and less
bulky display. In addition to flat CRT displays, other
20 flat panel displays, such as plasma displays, have also
been developed.

 In flat panel displays, a faceplate structure, a
backplate structure, and connecting walls around the
periphery of the faceplate and backplate structures
25 form an enclosure. In some flat panel displays, the
enclosure is held at vacuum pressure, e.g., typically 1×10^{-7} torr or less. The faceplate structure includes
an insulating faceplate and a light emitting structure
formed on an interior surface of the insulating
30 faceplate. The light emitting structure includes light
emissive elements such as phosphor or phosphor patterns
which define the active region of the display. The
backplate structure includes an insulating backplate
and electron-emitting elements located adjacent to the
35 backplate. The electron-emitting elements are excited
to release electrons which are accelerated toward the
phosphor, causing the phosphor to emit light which is

seen by a viewer at the exterior surface of the faceplate (the "viewing surface").

In vacuum pressure flat panel displays, a force is exerted on the faceplate and backplate structures of the flat panel display due to the differential pressure between the internal vacuum pressure and the external atmospheric pressure. If unopposed, this force can make the flat panel display collapse. The faceplate or backplate structure of a flat panel display may also fail due to external forces resulting from impacts sustained by the flat panel display.

Spacers have been used to internally support the faceplate and/or backplate structures. Previous spacers have been walls or posts located between pixels (phosphor regions that define the smallest individual picture element of the display) in the active region of the display.

Spacers have been formed by photopatterning polyimide. However, polyimide spacers may be inadequate because of: 1) insufficient strength; 2) inability to match the coefficient of thermal expansion of polyimide with the coefficient of thermal expansion of the materials typically used for the faceplate (e.g., glass), backplate (e.g., glass, ceramic, glass-ceramic or metal) and addressing grid (e.g., glass-ceramic or ceramic), resulting in breakage of the display; and 3) low required processing temperatures. With respect to item 3), the low processing temperature requirements prevent the use of higher process temperatures throughout the display assembly. The low temperature tolerance prevents the use of assembly methods and materials in the display that would otherwise be available. Examples of such methods and materials include: high reliability sealing frits, high temperature getter flash methods, and fast, high

temperature vacuum bake outs (which reduce manufacturing costs).

5 Spacers have also been made of glass. However, glass may not have adequate strength. Further, micro-cracks that are inherent in glass make glass spacers even weaker than "ideal" glass because of the tendency of micro-cracks to propagate easily throughout the glass spacers.

10 European Patent Publication 580 244 A1 describes glass spacers provided with the following items: (1) a high-ohmic material ($10^9 - 10^{14}$ ohms/square) coated on a spacer edge adjacent to the backplate structure (2) a patterned low-ohmic layer coated on a spacer edge adjacent to the backplate structure, (3) a conducting
15 layer coated on a spacer edge adjacent to the faceplate structure and (4) a coating having a low secondary emission coefficient formed over the entire spacer surface, including any layers provided by items (1), (2) and/or (3). The low secondary emission coefficient
20 coatings of item (4) include polyimide, titanium dioxide (TiO_2), or a suspension including chromium oxide (Cr_2O_3) particles, glass particles and an organic binder such as isopropanol.

25 For any spacer material, the presence of spacers may adversely affect the flow of electrons toward the faceplate structure in the vicinity of the spacers. For example, stray electrons may electrostatically charge the surface of a spacer, changing the voltage distribution near the spacer from the desired
30 distribution and resulting in distortion of the electron flow, thereby causing distortions in the image produced by the display.

35 It would therefore be desirable to have a spacer which is capable of adequately supporting and separating the faceplate and backplate structures while controlling the voltage distribution between these

structures. It would also be desirable to have a spacer having a thermal coefficient of expansion which can be matched to the thermal coefficients of expansion of the faceplate and backplate structures. It would
5 further be desirable to have a spacer which is easily manufacturable.

SUMMARY OF THE INVENTION

The invention provides structures and methods for
10 forming high strength spacers for use in flat panel displays. These spacers are positioned between a faceplate structure and a backplate structure of a flat panel display.

In one embodiment, an electrically resistive
15 spacer is formulated from a mixture of ceramic, such as aluminum oxide (alumina), which contains one or more transition metal oxides, such as titanium oxide (titania), chromium oxide (chromia), iron oxide or vanadium oxide. A wafer is fabricated from the ceramic
20 composition and fired. The wafer is given a desired electrical resistivity by controlling the time, temperature and kiln atmosphere during the firing step and by controlling the ratios of the transition metals to the other components of the ceramic composition.

25 Face metallization strips are formed along one or more of the outside surfaces of the wafer. After the metallization has been formed, the wafer is cut parallel to the face metallization strips to create the spacers.

30 As a result, the face metallization strips are positioned on the spacers immediately adjacent to the spacer edges which contact the faceplate and backplate structures. When the spacers are positioned between the faceplate and backplate structures, the face
35 metallization strips provide electrical contacts between the spacers and the faceplate and backplate

structures. This advantageously provides an even voltage distribution near the spacer ends.

Additionally, edge metallization strips can be formed over the spacer edges which contact the faceplate and backplate structures. The edge metallization provides an electrical connection between the spacers and the faceplate and backplate structures.

In another embodiment of the present invention, a spacer has an electrically insulating ceramic core with electrically resistive skins connected to the opposing outside surfaces of the spacer. The insulating ceramic core can be alumina, and the resistive skins can be formed from ceramic, such as alumina, containing a transition metal oxide, such as chromia, titania, iron oxide and/or vanadium oxide.

In one variation, a spacer is fabricated by forming a wafer from an electrically insulating ceramic and forming at least one additional wafer from an electrically resistive ceramic composition which includes an insulating ceramic and a transition metal oxide. The ceramic composition wafer may be thinner than the insulating ceramic wafer. The ceramic composition wafer is laminated on the outside surface of the insulating ceramic wafer to form a laminated wafer having electrically resistive skins. The laminated wafer is fired. After firing at the desired temperature and atmosphere, the wafer exhibits the desired electrical resistivity. Face metallization strips are formed on the outside surfaces of the laminated wafer. The resulting structure is cut along the face metallization strips to form the spacers. Edge metallization strips can also be added.

The electrical resistivity of the ceramic composition at the outside surface(s) of the spacers allows stray electrons to flow through this ceramic composition when a voltage is applied across the

spacers, thereby preventing charge build-up on the outside surfaces of the spacers. The formulation of the ceramic composition wafer can be chosen to have a low secondary electron emission to further reduce the charging effects. The strength of ceramic compositions, particularly those based on alumina is generally quite high, thereby reducing the number of spacers required in a display of a given size.

In another variation, a spacer is fabricated by forming an electrically resistive coating on an electrically insulating ceramic wafer. The insulating ceramic wafer is typically made of alumina, a filled glass or another ceramic composition. The electrically resistive coating can be insulating ceramic containing a transition metal oxide. The insulating ceramic wafer can be fired either before or after the electrically resistive coating is applied. Face metallization strips are fabricated on the outside surfaces of the resulting wafer structure. The resulting wafer structure is cut parallel to the face metallization strips to create the spacers. Edge metallization can also be added.

The electrical resistivity of the resistive coating at the outside surface(s) of the spacers allows stray electrons to flow through this resistive coating when a voltage is applied across the spacers, thereby preventing charge build-up on the outside surfaces of the spacers. A further advantage of the coating technique is that strength required of the spacer is provided by the ceramic core. This allows a broader selection of coating materials which may be selected to provide the desired combination of secondary electron emission and electrical resistivity to control the charging behavior of the spacer.

In yet another variation, the electrically insulating ceramic core of the spacer is formed from a

ceramic composition, such as alumina containing a transition metal oxide, wherein the transition metal oxide is present in the higher oxide states (i.e., a maximal valence oxide). Electrically resistive skins
5 are formed at the outside surfaces of the spacer by chemically reducing the outside surfaces of the spacer. By reducing the outside surfaces of the spacer, the coordination of the transition metal ions at these outside surfaces is altered, thereby causing the
10 transition metal oxide to become electrically resistive at the outside surfaces of the spacer. The spacer core remains electrically insulating. Face metallization strips are formed on the outside surfaces of the wafer, and a firing step is performed in a neutral atmosphere
15 on the resulting structure. The wafer is then cut parallel to the face metallization strips to form spacers. Edge metallization may be added.

The spacers described above, when used in a flat panel display, advantageously reduce power consumed by
20 the spacers while preventing charge build-up at the outside surfaces of the spacers. The thermal coefficients of expansion of the spacers can be controlled to achieve desired values by controlling the percentages of the materials used in the spacers. In
25 general, the wafer can be fired before or after the metallization is formed, depending upon the particular method used. The methods described above provide relatively simple and inexpensive techniques for the fabrication of the spacers.

30

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a perspective view of a wafer used to form spacers in accordance with the invention;

Figs. 2-4 are cross sectional views of a spacer
35 formed from the wafer of Fig. 1;

Figs. 5a-5d are cross sectional views illustrating a method of forming a spacer in accordance with one embodiment of the invention;

5 Fig. 6 is a perspective view of spacers positioned between a faceplate structure and a backplate structure;

Fig. 7 is a perspective view illustrating the connection of potential adjustment electrodes of a spacer to a power supply;

10 Fig. 8 is a perspective view of a laminated wafer having an electrically insulating core and electrically resistive skins;

Fig. 9 is a cross sectional view of a spacer formed from the laminated wafer of Fig. 8;

15 Fig. 10 is a perspective view of another wafer having an electrically insulating core and electrically resistive skins;

Fig. 11 is a cross sectional view of a spacer formed from the wafer of Fig. 10;

20 Fig. 12 is a perspective view of yet another wafer having an electrically insulating core and electrically resistive skins; and

Fig. 13 is a cross sectional view of a spacer formed from the wafer of Fig. 12.

25 In general, electrically conductive regions are illustrated with thin angled lines, electrically resistive regions are illustrated with alternating thick and thin angled lines, and electrically insulating regions are illustrated with thick angled lines.
30

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

The following definitions are used in the description below. Herein, the term "electrically
35 insulating" (or "dielectric") generally applies to materials having a resistivity greater than 10^{12} ohm-cm.

The term "electrically non-insulating" thus refers to materials having a resistivity below 10^{12} ohm-cm.

Electrically non-insulating materials are divided into (a) electrically conductive materials for which the resistivity is less than 1 ohm-cm and (b) electrically resistive materials for which the resistivity is in the range of 1 ohm-cm to 10^{12} ohm-cm. These categories are determined at low electric fields.

Examples of electrically conductive materials (or electrical conductors) are metals, metal-semiconductor compounds, and metal-semiconductor eutectics. Electrically conductive materials also include semiconductors doped (n-type or p-type) to a moderate or high level. Electrically resistive materials include intrinsic and lightly doped (n-type or p-type) semiconductors. Further examples of electrically resistive materials are cermet (ceramic with embedded metal particles) and other such metal-insulator composites. Electrically resistive materials also include conductive ceramics and filled glasses.

Spacers of the invention can be utilized to separate the faceplate and backplate structures in a flat cathode ray tube (CRT) display. A faceplate structure typically includes an electrically insulating faceplate with a light emitting structure located on an interior surface of the faceplate. The backplate structure typically includes an electrically insulating backplate with an electron emitting structure located on an interior surface of the backplate.

Spacers in accordance with the invention can also be used in other flat panel displays such as plasma displays or vacuum fluorescent displays. Further, these spacers are not limited to use in displays, but can be used in other flat panel devices used for purposes such as optical signal processing, optical addressing in devices such as phased array radar

devices, or in devices, such as copiers or printers, which scan an image to be reproduced on another medium. Additionally, the invention is applicable to flat panel devices having non-rectangular screen shapes, e.g.,
5 circular, and irregular screen shapes such as might be used in a vehicle dashboard or an aircraft control panel.

Herein, a flat panel display is a display in which the faceplate and backplate structures are
10 substantially parallel, and the thickness of the display is small compared to the thickness of a conventional deflected-beam CRT display, the thickness of the display being measured in a direction substantially perpendicular to the faceplate and
15 backplate structures. Typically, though not necessarily, the thickness of a flat panel display is less than 5 cm. Often, the thickness of a flat panel display is substantially less than 5 cm -- e.g., 0.5 - 2.5 cm.

20 Spacers of the invention can be used in flat panel displays such as those described in more detail in commonly owned PCT International Application Numbers PCT/US94/00602, PCT/US94/09762, and PCT/US95/00555, the pertinent disclosures of which are incorporated by
25 reference herein.

There are several methods of producing spacers in accordance with the invention. These methods include (1) manufacturing a spacer from a solid piece of uniform electrically resistive material such as a
30 ceramic containing a transition metal oxide or a filled glass system in which the glass is made electrically resistive by the addition of a transition metal oxide and the fillers are chosen to provide the desired electron emission and thermal expansion match, (2)
35 manufacturing a spacer by laminating electrically resistive skins on outside surfaces of an electrically

insulating core, (3) manufacturing a spacer from an electrically insulating ceramic composition, wherein electrically resistive skins are formed at the outside surfaces of the spacer by reducing the outside surfaces of the ceramic composition, and (4) manufacturing a
5 spacer by coating an electrically resistive material on an electrically insulating core.

In Method (1) listed above, spacers are formed from a solid piece of uniform electrically resistive
10 material. In one embodiment, the uniform resistive material is an electrically resistive ceramic composition formed by adding a transition metal oxide such as iron oxide, titania, chromia, vanadium oxide or nickel oxide to an electrically insulating ceramic such
15 as alumina. The addition of a transition metal oxide to the alumina results in a ceramic which has an electrical resistivity in the desired range of 10^5 to 10^{10} ohm-cm.

When adding titanium or iron to alumina, the
20 replacement of as few as 4% of the aluminum cations in the alumina results in a resistivity in the desired range (i.e., 10^5 to 10^{10} ohm-cm). Because of the small amount of titanium or iron required, the thermal coefficient of expansion (TCE) of the resulting
25 composition is essentially the same as the TCE of alumina.

A larger amount of chromium is added to alumina to provide an electrical resistivity in the desired range. As a higher percentage of chromia is added to the
30 ceramic composition, the effective inter-cation distance in the resulting lattice structure decreases. This decreased inter-cation distance increases the overlap of electrons in the lattice structure, thereby forming a composition having the desired electrical
35 resistivity. A ceramic including alumina and chromia can contain up to 90% chromia by weight.

The use of chromia advantageously results in a ceramic having a low secondary electron emission. For example, a ceramic composition of alumina and chromia can have a secondary electron emission of less than two at 2 kV. This advantageously reduces the voltage deviation around the spacers.

By controlling the relative amounts of chromia and alumina, the TCE of the resulting ceramic composition can be controlled to be any value between the TCE of alumina (approximately 72) and the TCE of chromia (approximately 84). In certain embodiments, silicon dioxide (silica) is added to the alumina and chromia to keep the TCE near 70. Alumina and chromium sesquioxide (Eskolaite) are known to form a continuous range of solid solutions all having the corundum crystal structure. X-ray diffraction studies have shown that the crystal structure can be maintained as corundum even while accommodating up to 20% admixtures of silica. Other transition metal oxides, such as oxides of iron or vanadium can be used to create the electrically resistive ceramic composition.

In Method (1), spacers are fabricated from a slurry created by mixing ceramic powders, organic binders and a solvent in a conventional ball mill. In a particular embodiment, this slurry is a ceramic composition which includes 90% alumina and 10% titania (hereafter, the "90/10 alumina-titania composition"). Table 1 sets forth a formula for such a slurry.

Table 1

30

Alumina powder	292 grams
Titania powder	32 grams
Butvar B76	34 grams
Santicizer 150	10 grams
Kellogg Z3 Menahden oil	0.65 gram
Ethanol	105 grams

35

Toluene	127 grams
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5 In another embodiment, the slurry is a ceramic composition which includes 2% titanium, 34.3% alumina and 63.7% chromia (hereafter, the "2/34/64 composition"). Table 2 sets forth a formula for such a slurry.

10 Table 2

Alumina powder	111.1 grams
Chromia powder	206.4 grams
Titania powder	6.48 grams
Butvar B76	34 grams
15 Santicizer 150	10 grams
Kellox Z3 Menahden oil	0.65 gram
Ethanol	105 grams
Toluene	127 grams

20 In other embodiments, the ceramic formula also contains modifiers chosen to control grain size or aid sintering. Compounds such as silicon dioxide, magnesium oxide, and calcium oxide can be used as modifiers.

25 Using conventional methods, the milled slurry is used to cast a tape having a thickness of 110-120 μm . In one embodiment, this tape is cut into large wafers which are 10 cm wide by 15 cm long. The wafers are then loaded onto a flat conventional setter and fired
30 in air and/or a reducing atmosphere until the wafers exhibit the desired resistivity.

In particular, the wafers are typically fired in a cold wall periodic kiln using a hydrogen atmosphere with a typical dew point of 24°C. If the organic components of the wafer are to be pyrolyzed (i.e., removed) in the same kiln, the dew point of the hydrogen atmosphere will be higher (approximately 50°C) to facilitate removal of the organics without damaging the wafers. The dewpoint will be shifted from the higher dew point (50°C) to the lower dewpoint (24°C) after the organic components of the wafer are pyrolyzed. Pyrolysis is typically complete at a temperature of 600°C. Typically, the wafers are fired at a peak temperature of 1620°C for 2.5 hours. The properties of the ceramic composition are controlled by the detailed firing profile. Depending on the starting raw materials, and on the exact combination of strength, stability, resistivity, and secondary electron emission desired in the spacer, the actual peak temperature may be between 1450°C and 1750°C, and the firing profile may maintain this peak temperature from 1 to 16 hours.

The wafers are then unloaded and inspected. For the 90/10 alumina-titania composition, the measured TCE of the resulting wafers was 71.6. The resulting wafers had a sheet resistance of approximately 10^8 ohm-cm. The 2/34/64 composition results in a resistance of approximately 2×10^8 ohm-cm.

Next, stripes of metal are formed on at least one face of the wafer. These face metal stripes will serve as electrodes on the face of the resulting spacer. Face metal stripes may be put down by any of a number of suitable techniques such as evaporation, sputtering, photolithography, electroplating, screen printing, direct pen writing, or by decomposition of an organometallic material with a laser beam.

If, for example, the face metal stripes are fabricated by evaporation, the following steps would be appropriate. The wafer is first masked so that the evaporated metal will fall only on the desired portions of the face of the wafer. The masked wafer is placed in a vacuum chamber (not shown). The vacuum chamber contains an arrangement of containers which may be heated so that a metal (e.g., chromium, nickel or aluminum) placed within the containers is vaporized at low pressure. The mean free path of the metal atoms in the vapor under such conditions is long enough that the metal atoms impinge on the exposed surface of the substrate with considerable force, thereby promoting adhesion of the metal atoms with the exposed face of the wafer. Thus, a metal stripe is formed on the surface of the wafer wherever there is an opening in the mask. The evaporation conditions depend upon the metal chosen to form the stripes and the condition of the wafer surface. The evaporation temperature is typically in the vicinity of 1000°C, and the time to effect the evaporation is less than a minute. The vacuum evaporation apparatus typically has a port and other means by which the parts may be rapidly introduced into the chamber and the supply of metal replenished.

The mask can be made by standard photolithographic techniques. Such techniques allow fine metal stripes to be fabricated, especially during the fabrication of non planar spacer structures. In photolithographic techniques, the wafer is first coated with a commercial photoresist and the photoresist is cured. The cured resist is exposed by projection of the desired stripe pattern onto the surface. The surface of the wafer is exposed by washing away the unexposed photoresist. The wafer thus prepared is placed into the vacuum evaporator. Metal is evaporated onto the wafer surface

in the manner previously described. The metallized wafer is removed from the chamber and the photoresist is chemically removed. During the photoresist removal, the metal lying on the photoresist is lifted off so
5 that the metal electrode stripes are left on the face of the wafer.

Fig. 1 illustrates a wafer 100 having face metallization strips 101-105 located on outside surface 112 and face metallization strips 106-110 formed on
10 outside surface 114. Wafer 100 is greatly magnified for purposes of illustration. In one embodiment, there are 1140 face metallization strips, each having a width of 0.0025 mm. The face metallization strips on surface 112 are aligned with the face metallization strips on
15 surface 114. For example, strip 103 is situated substantially opposite strip 108. The center-to-center spacing between each of these face metallization strips is typically 0.5 mm. As discussed below, this center-to-center spacing defines the spacer height.

20 The face metal stripes may also be applied by using materials similar to the thick film metallizations widely used to prepare hybrid circuits. These metallization materials consist of a mixture of a metal powder and powdered glass or other material that
25 promotes adhesion of the metal to the ceramic. The metallization materials are suspended in an organic binder that allows the combination to be deposited by any of a variety of common printing techniques. Stripes of this material may be applied through masks
30 similar to those used for evaporation, by screen printing or by direct application of the stripes using a special pen. In all cases, the material must be fired to fuse the metal powder into a conductor and simultaneously bond the material to the ceramic. The
35 oxidation state of the ceramic materials employed in the wafer is crucial in determining the resistivity and

charging behavior of the spacer. Maintaining this material in the proper oxidation state may require that the firing of the electrode metallization be carried out in a neutral or reducing atmosphere. Typically, thick film metallization materials are designed to fire at temperatures between 800°C and 1000°C. While not all thick film metallizations are compatible with firing in atmospheres other than air, almost all manufacturers of these materials offer products specifically compounded for such firing.

Wafer 100 is subsequently cut along face metallization strips 101-110 to form spacers. Lines 121-123 indicate the locations of the cuts. This cutting step can be performed using a conventional saw having a diamond impregnated blade.

Fig. 2 illustrates a typical spacer 140 corresponding to the lowermost strip created after cutting along line 123 of wafer 100 (Fig. 1). Spacer 140 has outside surfaces 112 and 114 and edge surfaces 126 and 128.

Edge metallization strips can be applied to the edge surfaces of each spacer. Fig. 3 depicts spacer 140 after edge metallization strips 130 and 131 are applied to edge surfaces 126 and 128. Edge metallization strips 130 and 131 are applied using conventional techniques.

Methods similar to those used for application of metal to the face of the wafer can be used to apply edge metallization strips 130 and 131. While there are differences in the fixturing required to orient the spacers so as to confine the metal to the edges, the process of applying the metallization material is only slightly altered. As a practical matter, in applying metal to the edges it is usual to gather the cut spacers into large blocks so that many may be processed at one time. Edge metallization has been placed on

spacers by evaporating aluminum on the spacer edges and by screen printing silver, tungsten, or molybdenum-manganese on the spacer edges. Edge metallization has also been placed on spacers by
5 combining silver or palladium with an organometallic material, screen coating the combination on the spacer edges, and thermally decomposing the combination at temperatures near 450°C.

After edge metallization strips 130 and 131 are
10 formed, the resulting spacer structure can be fired in accordance with conventional techniques. Final inspection is performed to complete the fabrication of spacer 140.

Fig. 4 depicts metal potential adjustment
15 electrodes 161-162 formed on outside surface 112 of spacer 140. Potential adjustment electrodes 161-162 are typically formed at the same time that face metallization strips 101-110 are formed. Potential adjustment electrodes 161-162 are approximately 0.025
20 mm wide. In a particular embodiment, spacer 140 has a height of approximately 1.27 mm, potential adjustment electrode 161 is located approximately 0.25 mm from electron emitting structure 172, and potential adjustment electrode 162 is located 0.76 mm from
25 electron emitting structure 172. Edge metallization strip 130 contacts light emitting structure 171 of faceplate 174. Edge metallization strip 131 contacts electron emitting structure 172 of backplate 175.

The voltages of light emitting structure 171, edge
30 metallization strip 126, and face metallization strips 104 and 109 are controlled by a power supply circuit 180, which is connected to at least two of the electrodes formed on outside surface 112. Power supply circuit 180 is a conventional element which can take
35 various forms. In Fig. 4, power supply circuit 180 is connected to face metallization electrodes 104 and 105,

as well as potential correction electrodes 161 and 162. Power supply circuit 180 provides a first voltage V1 to face metallization electrode 104, a second voltage V2 to potential correction electrode 162, a third voltage V3 to potential correction electrode 161 and a fourth voltage V4 to face metallization electrode 105, wherein $V1 > V2 > V3 > V4$. Spacer 140 is sufficiently thin that potential correction electrodes 161-162 control the voltage distribution at opposite surface 114. In alternate embodiments, potential correction electrodes are also included on surface 114.

In an alternate embodiment, power supply circuit 180 provides only a first voltage V1 to face metallization electrode 104 and a second voltage V4 to face metallization electrode 105. In such an embodiment, the voltages existing on potential correction electrodes 161-162 are determined by the voltage divider circuit created by potential correction electrodes 161-162 and spacer 140. That is, the voltages on potential correction electrodes 161-162 are determined by the resistance of the portion of spacer 140 located between electrodes 104 and 162, the resistance of the portion of spacer 140 located between electrodes 162 and 161, and the resistance of the portion of spacer 140 located between electrodes 161 and 105.

Potential adjustment electrodes 161-162 control the voltage distribution along spacer 140. Stray electrons which strike outside surfaces 112 and 114 of spacer 140 travel to potential adjustment electrodes 161-162, thereby preventing charge build-up at the outside surfaces 112 and 114 of spacer 140. Power supply circuit 180 is typically connected at the ends of spacer 140 which extend outside of the active regions of the faceplate and backplate structures 174 and 175.

Figs. 5a-5d illustrate a variation of Method (1). As illustrated in Fig. 5a, wafer 201 is attached to glass substrate 200 with an adhesive 202. In one embodiment, adhesive 202 is wax-based bonding material. 5 Face metallization layer 203 is formed on wafer 201 by sputtering, evaporation or chemical deposition before wafer 201 is attached to glass substrate 200.

Face metallization layer 203 is patterned using conventional photolithographic methods to create face 10 metal electrodes 205 (Fig. 5b). Face metal electrodes 205 are then coated with a protective film 206 (Fig. 5b). A layer of photoresist can be used to form protective film 206.

Wafer 201 is then sawed into strips 207 (Fig. 5c). 15 In one embodiment, strips 207 have a length L of 1.27 mm and a height H of 0.064 mm.

Metal is then formed on the exposed edges of strips 207 by sputtering, evaporation or chemical deposition to form edge metal electrodes 208 (Fig. 5d). 20 Protective film 206 and adhesive 202 are dissolved, thereby separating strips 207 from glass substrate 200. Strips 207 are then cleaned (e.g., ultrasonically).

In another variation of Method (1), the green (unfired) ceramic is slit into strips. The organic 25 elements of the unfired ceramic tape render the tape plastic and capable of being handled in similar fashion to conventional plastic sheet materials. Thus, the slitting can be accomplished by feeding the unfired ceramic sheet through a conventional slitter similar to 30 equipment used in the fabrication of paper and plastic products. These strips are then fired in specially designed fixtures to form the spacers. The fired strips can be metallized in a similar fashion to the wafer described above.

35 In another variation of this method, the metallization may be a metal chosen to be compatible

with the high firing temperature required to convert the green wafer to ceramic. This technique, known as cofiring, has been used to fabricate packages for mounting semiconductor integrated circuit devices.

5 Metals used for cofiring include tungsten and molybdenum at high temperatures. Copper and silver can be cofired with low temperature glass ceramics. Wafers with stripes of metal applied in the green (unfired) state can be fabricated either into fired wafers which
10 are subsequently cut into individual spacers, or cut into strips along the metallized stripes and fired as individual spacers.

Fig. 6 illustrates spacers 340 and 341 positioned between faceplate structure 350 and backplate structure
15 351 of a flat panel CRT display. Face metallization strips 330-333 adjoin faceplate structure 350, and face metallization strips 334-337 adjoin backplate structure 351. Faceplate structure 350 includes faceplate 302 and light emitting structure 306. Backplate structure
20 351 includes backplate 303 and electron emitting structure 305. Illustratively, the internal surfaces of faceplate 302 and backplate 303 are typically 0.1 - 2.5 mm apart. Faceplate 302 is glass having, illustratively, a thickness of 1.0 mm. Backplate 303
25 is glass, ceramic, or silicon having, illustratively, a thickness of 1.0 mm. The center-to-center spacing of spacers 340 and 341 is, illustratively, 8 to 25 mm along dimension 316.

Electron emitting structure 305 includes electron-
30 emissive elements (field emitters) 309, a patterned metallic emitter electrode (sometimes referred to as a base electrode) divided into a group of substantially identical straight emitter electrode lines 310, a metallic gate electrode divided into a group of
35 substantially identical straight gate electrode lines 311, an electrically insulating layer 312 and focusing

ridges 380. Other types of electron emitting structures can be used with the spacers of the invention.

5 Emitter electrode lines 310 are situated on the interior surface of backplate 303 and extend parallel to one another at a uniform spacing. Insulating layer 312 lies on emitter electrode lines 310 and on laterally adjoining portions of backplate 303. Gate electrode lines 311 are situated on insulating layer
10 312 and extend parallel to one another (and perpendicular to emitter electrode lines 310) at a uniform spacing.

Field emitters 309 are distributed in an array above the interior surface of backplate 303. In
15 particular, each group of field emitters 309 is located above the interior surface of backplate 303 in part or all of the projected area where one of gate lines 311 crosses one of emitter lines 310. Spacers 340 and 341 extend towards areas between field emitters 309 and
20 also between emitter electrode lines 310.

Each group of field emitters 309 extends through an aperture (not shown) in insulating layer 312 to contact an underlying one of emitter electrode lines 310. The tops (or upper ends) of each group of field
25 emitters 309 are exposed through a corresponding opening (not shown) in an overlying one of gate electrode lines 311. Field emitters 309 can have various shapes such as needle-like filaments or cones.

Focusing ridges 380, which extend above gate lines
30 311, are electrically isolated from gate lines 311. Focusing ridges 380 are described in more detail in International Application Number PCT/US95/00555, cited above. Spacers 340 and 341 (and face metallization strips 334-337) contact focusing ridges 380. In this
35 case, face metallization strips 334-337 abut focusing ridges 380 and are held at the same potential as

focusing ridges 380. An electrically conductive material (not shown) can also be located outside the active area of backplate structure 351 to provide an electrical connection between face metallization strips 334-337 and focusing ridges 380. This electrical connection prevents charge build-up near the ends of spacers 340 and 341 adjacent electron emitting structure 305. In alternate embodiments, spacers 340 and 341 include edge metallization strips (not shown).

Light emitting structure 306 is situated between faceplate 302 and spacers 340 and 341. Light emitting structure 306 consists of a group of light emissive regions 313 (e.g., phosphor) that produce light when struck by electrons, a black matrix of substantially identical dark, non-reflective ridges 314 that do not produce light when struck by electrons, and a light reflective layer 315. Light emissive regions 313 are divided into a plurality of substantially identical regions 313r, 313g and 313b that emit red (R), green (G) and blue (B) light, respectively.

Light reflective layer 315 and, consequently, light emissive regions 313 are maintained at a positive voltage of 1500 - 10,000 volts relative to the voltage of field emitters 309. When one group of field emitters 309 is suitably excited by appropriately adjusting the voltages of emitter electrode lines 310 and gate electrode lines 311, that group of field emitters 309 emits electrons which are accelerated towards a target light emissive region 313. Fig. 6 illustrates trajectories 317 followed by one such group of electrons. Upon reaching the target light emissive region 313, the emitted electrons cause these phosphors to emit light 318.

Some of the electrons invariably strike parts of the light-emitting structure other than the target phosphors. As illustrated by trajectory 317a, some

electrons strike the spacers. The black matrix formed by dark ridges 314 compensates for off-target hits in the row direction to provide sharp contrast as well as high color purity.

5 Light reflective layer 315, typically aluminum, is situated on light emissive regions 313 and dark ridges 314 as shown in Fig. 6. The thickness of light reflective layer 315 is sufficiently small that nearly all of the emitted electrons that strike layer 315 pass
10 through layer 315 with little energy loss. The surface portions of layer 315 adjoining light emissive regions 313 are quite smooth so that part of the light emitted by regions 313 is reflected by layer 315 through faceplate 302. Light reflective layer 315 also acts as
15 the anode for the display. Because light emissive regions 313 contact layer 315, the anode voltage is impressed on regions 313.

Spacers 340 and 341 contact light reflective layer 315 on the anode side of the display. Because dark
20 ridges 314 extend further toward backplate 303 than light emissive regions 313, spacers 340 and 341 contact portions of layer 315 along the tops (or bottoms in the orientation shown in Fig. 6) of ridges 314. The extra height of ridges 314 prevents spacers 340 and 341 from
25 contacting and damaging light emissive regions 313. Face metallization strips 330-333 abut layer 315 and are therefore electrically connected to layer 315.

An electrically conductive material (not shown) can also be located outside the active area of
30 faceplate structure 350 -- i.e., around the outer edges of faceplate structure 350 -- to provide an electrical connection between face metallization strips 330-333, and layer 315. For example, face metallization strips 330-333 and layer 315 can extend to the outer edges of
35 faceplate structure 350 to be electrically connected to an electrically conductive frit. The frit is a glass

composite material which bonds the outer edges of faceplate structure 350 to the flat panel display. The frit is made electrically conductive by including metal particles in the glass composite material.

5 The electrical connections between face metallization strips 330-333 and layer 315 cause face metallization strips 330-333 to be biased at the same high voltage as layer 315. As a result, stray electrons which strike the surface of spacers 340 and
10 341 near face metallization strips 330-333 travel to face metallization strips 330-333. In this manner, charge build-up is prevented near the ends of spacers 340 and 341 adjacent light emitting structure 306.

Electrically conductive frit material can also be
15 used to connect potential adjustment electrodes or face metallization strips to a power supply. Fig. 7 illustrates the connection of potential adjustment electrodes 701 and 702 of spacer 700 to power supply circuit 703 in accordance with the invention.
20 Potential adjustment electrodes 701 and 702 extend along spacer 700 outside of the active region of the flat panel display. Potential adjustment electrodes 701 and 702 then extend to one of the edge surfaces of spacer 700. Portions of electrically conductive frit
25 material 715 and 716 connect electrodes 701 and 702 to electrodes 711 and 712 on substrate 721 of the backplate structure 720. Electrodes 701 and 702 connect to power supply circuit 703, thereby applying the desired voltages to potential adjustment electrodes
30 701 and 702. Frit portions 715 and 716 also help to support spacer 700. Frit 715-716 can be formed by various methods including screen printing and conventional photolithographic techniques.

Alternatively, one or both of electrodes 701 and
35 702 extend to the other edge surface of spacer 700 and are connected with frit material to corresponding

electrodes on a faceplate structure (not shown). In other variations, face metallization strips (not shown) on spacer 700 are connected to electrodes formed on the faceplate or backplate structure in the manner previously described.

Turning now to Method (2), spacers are fabricated by laminating electrically resistive skins onto outside surfaces of an electrically insulating core. Fig. 8 depicts a laminated wafer 400 formed with an insulating ceramic core 401 and electrically resistive skins 402 and 403. In one embodiment, insulating core 401 is formed from an alumina ceramic tape having a thickness of 7.5-75 μm . The alumina core ceramic is prepared by first dispersing alumina powder in an organic material such that a homogenous distribution of the alumina powder in the organic material is achieved. The dispersion can be carried out in a ball mill, vibratory mill, planetary mill or other apparatus known to those skilled in the art. The dispersed powder organic mix is formed into tape by a process such as tape casting or roll compaction. In tape casting, the organic slurry is carried under a doctor blade to level a thin film to a uniform height. By careful control of the solvents and other organic constituents, this film of slurry can be made to dry to a uniform film of a precise thickness. Another method of preparing tape is to form the dispersed powder slurried in the organic mix into a tape by passing slurry through a pair of rollers. These rollers squeeze the tape to a uniform thickness. This is commonly called roll compaction. Feedstocks for roll compaction may also be formed by spraying the ceramic powder dispersed in a binder and solvent mix into a special drying chamber. This process forms large particles of the powder and binders. By choice of proper ratios for the particular particle morphology of the powder this "spray dried"

powder can be made free flowing. This free flowing powder forms a convenient feedstock for the roll compaction process.

5 The 90/10 alumina-titania composition and the 2/34/64 composition discussed in connection with Method (1) are suitable for use as electrically resistive skins 402 and 403 in Method (2). There are a large number of other compositions suitable for use as electrically resistive skins 402-403. Any of the
10 compositions previously described in connection with Method (1) may be used. Compositions that cannot be used to fabricate uniform electrically resistive spacers by reason of strength or uniformity can be used to fabricate electrically resistive skins 402-403. As
15 a result, the composition range is wider for resistive skins 402-403. The objective is to formulate a material with an electrical resistivity in the proper range and a low and controllable secondary electron emission.

20 Solid solutions of chromium and aluminum oxides are particularly useful. These compositions require firing in carefully controlled atmospheres. The conduction mechanism of such solid solutions is complex. Since the chromium and alumina form a solid
25 solution, the separation between chromium cations is too great for easy transfer of the electrons between them. The charge carrier is therefore supplied by a small admixture of titanium dioxide. Titanium dioxide (titania) also aids the sintering of chromium
30 sesquioxide by stabilizing the oxidation states. The reaction of titania to the reducing atmospheres needed to fire the chromia-alumina solid solution reduces the titania to a lower oxide state. This not only aids in the sintering of the body, but also provides the needed
35 conductivity by partially reducing the oxidation state of the titania.

The solubility of the titania in the crystals of chromia-alumina solid solution is limited to approximately 2%. As a result, at concentrations greater than 2%, the majority of the titania is exuded to the grain boundaries of the material as the crystals grow during the sintering operation. Thus, the concentration of the titania is quite high in the more disordered material at the grain boundaries. The volume fraction of the material occupied by this less ordered material is small compared to that of the grains of crystalline solid solution. However, since the material is rich in titania, the transfer of electrons between titanium cations of varying coordination is easy compared to that in the crystalline material that forms the bulk of the solid. Therefore the charge transport is mostly through the grain boundary materials in these compositions.

The secondary electron generating properties of the titania-chromium-alumina solid solutions are quite close to those of the pure chromium oxide which produces a desirable low charging current in spacers made of these materials, while the conductivity on the grain boundaries may be manipulated over a wide range by varying the admixture of titania.

The sintering behavior of the titania-chromium-alumina materials is complex. To make a suitable spacer the proper ratio of grain volume to grain boundary volume must be maintained while controlling not only the composition of the solid solution, but also the composition of the grain boundary. The firing conditions, particularly the peak temperature, the partial pressure of oxygen in the kiln atmosphere, the firing ramps, and the firing times must be appropriate to the particular composition being processed. Composition ranging from 10% chromium sesquioxide and 90% alumina to 90% chromium and 10% alumina have been

made. These compositions have all been modified with 0.25% to 8% titanium dioxide. The kiln atmospheres have ranged from 10^{-20} atm oxygen partial pressure as water vapor in a hydrogen atmosphere to 3% oxygen as water vapor in a mixture of 20% hydrogen 80% nitrogen.

In one embodiment, the 2/34/64 composition is cast into a tape having a thickness of approximately 0.05 mm.

The alumina tape is cut into wafers to form insulating cores, such as insulating core 401. Similarly, the 2/34/64 composition tape is cut into wafers to form electrically resistive skins, such as skins 402 and 403. Insulating core 401 and resistive skins 402 and 403 have approximately the same length and width measurements. For example, insulating core 401 and resistive skins 402-403 can each be approximately 10 cm wide and 15 cm long.

The spacer is formed of a laminate of resistive skins 402 and 403 on either side of insulating ceramic core 401. The layer thicknesses are chosen so that the completed laminate will have the desired spacer thickness. In one embodiment, spacers are made by laminating 0.0127 mm thick resistive skins to a 0.3175 mm thick ceramic core. The layers can be laminated by continuously feeding strips of the three unfired layers 401-403 through metal rollers adjusted to provide sufficient heat and pressure to fuse the green material. This provides a continuous and low cost method for fabricating the laminate. At a temperature of approximately 100°C, the unfired layers 401-403 easily fuse when passing through the rollers. As a result, laminated wafer 400 is formed.

The remaining process steps of Method (2) -- e.g., forming face and/or edge metallization strips -- are similar to the steps previously described in connection with Method (1). However, in Method (2), the step of

firing wafer 400 in a reducing atmosphere is performed such that laminated wafer 400 experiences a greater degree of reduction. This advantageously reduces the electrical resistivity of resistive skins 402 and 403 without significantly decreasing the bulk resistivity of the spacer. The desired electrical resistivity of resistive skins 402 and 403 is 10^5 - 10^{10} ohm-cm.

Fig. 9 illustrates a spacer 404 formed by Method (2). Spacer 404 includes portions of insulating core 401 and electrically resistive skins 402 and 403. Spacer 404 includes face metallization strips 405 and 406 on outside surface 407 of resistive skin 402, and face metallization strips 408 and 409 on outside surface 410 of resistive skin 403. Spacer 404 also includes edge metallization strip 412 formed on edge surface 414 and edge metallization strip 416 formed on edge surface 418. Spacer 404 can also be fabricated with only face metallization strips 405-406 and 408-409 or only edge metallization strips 412 and 416.

The total thickness of the laminated spacer formed by Method (2) is approximately the same as the thickness of the solid spacer formed by Method (1). Resistive skins 402 and 403 can be cast at a minimum thickness of 70-80 μ m.

Laminated spacer 404 formed by Method (2) advantageously exhibits a high bulk resistivity because of the insulating characteristics of core 401. The strength of laminated spacer 404 is approximately equal to the strength of the material used to fabricate insulating core 401 (e.g., alumina). Furthermore, the steps set forth in connection with Method (2) make it relatively easy to control the sheet resistance of skins 402 and 403.

Additionally, because skins 402 and 403 are thin and separated by insulating core 401, defects such as pinholes are not as important as they are for spacers

of solid construction. A small pin hole does not adversely affect the operation of spacer 404 for two reasons. One reason is that a hole which is smaller in diameter than the thickness of skins 402 and 403 still
5 effectively shields insulating core 401 from the electrons which are transmitted between the faceplate and backplate structures. The other reason is that the strength and other performance factors of spacer 404 are largely unaffected by small defects in skins 402
10 and 403 since such defects terminate at core 401 and therefore can not propagate through core 401 to cause failure of spacer 404.

In variations of Method (2), laminated wafers such as laminated wafer 400 are fabricated with skins made
15 of other ceramic compositions which include ceramics containing transition metal oxides. There are many compositions which are suitable for such spacers. In addition to the transition metal oxide compositions previously described, there are compositions containing
20 copper (e.g., copper oxide), families of chalcogenides, and semiconductors with resistivities in the proper range.

Turning now to Method (3), the electrically insulating ceramic core of the spacer can be formed
25 from a ceramic composition, such as alumina containing a transition metal oxide, wherein the transition metal oxide is present in the higher oxide states. Electrically resistive skins are formed at the outside surfaces of the spacer by chemically reducing the
30 outside surfaces of the spacer. By reducing the outside surfaces of the spacer, the coordination of the transition metal ions at these outside surfaces is altered, thereby causing the transition metal oxide to become electrically resistive at the outside surfaces
35 of the spacer. The spacer core remains electrically insulating. The reducing step can be performed in a

number of different ways, including firing the spacer in a reducing atmosphere, or exposing the spacer to a laser beam, charged particles or photon irradiation.

5 Spacers fabricated in accordance with Method (3) are formed from a ceramic composition which is formulated such that the electrical resistivity of the composition can be altered by selective reduction. The ceramic composition is selected such that the resistivity of the composition is a function of the
10 oxidation state of at least one component of the composition. The ceramic composition is also selected such that the crystal structure of the composition allows the electrical resistivity of the composition to be altered by selective reduction of the surface of the
15 composition. Compositions which exhibit these properties include glasses containing transition metal oxides, non-centrosymmetric titanates such as barium titanate, lead titanate and bismuth titanate. Mixtures of these compositions can also be used. Commercial
20 materials, such as iron and chromium containing glasses (typically used as glazes for high voltage insulator strings), can also be used.

 In each of the above listed compositions, the resistivity is determined by the ratio of the
25 transition metal cations in one coordination to the transition metal cations in another coordination. For example, in a composition in which titanium cations are the charge carriers, the ratio of Ti^{3+} to Ti^{4+} cations determines the resistivity of the composition.
30 Similarly, in a composition in which vanadium cations are the charge carriers, the ratio of V^{4+} to V^{5+} cations determines the resistivity. The superscripted numbers indicate the number of nearest neighbor oxygen anions. By altering these ratios, the resistivity of the
35 compositions are changed. By controlling the oxide states of these compositions, a spacer can be

fabricated having a core with a resistivity which is much higher than a resistivity of the outer surfaces of the spacer.

5 It is important that the transition metal cation be bound in the composition such that the oxidation state of the cation can be altered by a displacive (rather than reconstructive) transformation of the crystal lattice of the composition. The displacive transformation is effected at temperatures well below
10 the melting point of the material, but substantially above the temperature the spacer will experience during normal use in a flat panel display. Consequently, the electrical properties of the composition remain stable during use.

15 One method of formulating a suitable ceramic composition is to dissolve a transition metal in a silicate glass. The transition metal cations provide the charge carriers to provide electrical conductivity. The number of charge carriers present in the material
20 depends on the ratio of the cations in the two relevant coordinations (e.g., Ti^{3+} and Ti^{4+} in the case of titanium). The number of cations in each coordination is a function of the total oxidation state of the composition. If this oxidation state is altered, the
25 conductivity is also altered. A glass or glass ceramic containing transition metal ions may be altered by oxidation or reduction at low temperatures if the crystal structure permits displacive transformation of the cation coordination. Thus, a transition metal
30 oxide glass can serve as the spacer, or the glass may be filled with other ceramic components to produce a material with a TCE and secondary electron emission tailored to particular values.

If the transition metal oxide is dispersed in a
35 very stable crystal, it is very difficult to alter the coordination of the cations. To substantially reduce

the electrical resistivity of such a crystal, high temperature reconstructive transformations must be induced. A chromia-alumina solid solution provides an example of a stable crystal which must undergo
5 reconstructive transformation to reduce the resistivity of the solid solution.

After selecting a ceramic composition which allows alteration of the oxide state via a displacive transformation, the spacer is formed and fired in a
10 manner similar to that previously described in connection with Method (1). The firing atmosphere is dictated by the selection of the oxide system which provides the conduction. For example, if titanium or iron is selected as the active cation, then an initial
15 firing step is carried out in air. This air firing would place most of the titanium or iron cations in higher coordination sites (e.g., Ti^{4+}). Thus, the ratio of cations in the lower coordination sites (e.g., Ti^{3+}) to those in the higher coordination sites (e.g., Ti^{4+})
20 is low. Consequently, the resulting composition is electrically insulating.

A conductive layer is formed on the outer surface of the composition by a second firing in a reducing atmosphere. This second firing creates vacancies in
25 the anion lattice surrounding some of the titanium or iron cations. As a result, the ratio of Ti^{3+} to Ti^{4+} cations (assuming titania is used) is raised and the composition becomes more conductive at the outer surface. The depth of these electrically resistive
30 skins can be controlled by choosing a proper combination of firing time and temperature. For example, resistive skins have been formed on air fired lead barium titanate compositions by exposure to 10% hydrogen, 90% nitrogen atmospheres for eight hours at
35 950°C. After the resistive skin has been formed on a

wafer, the wafer can then be metallized and cut to form the spacers.

The thickness and resistivity of the resistive skins can be selected to reduce the power dissipated in the spacer, or allow the use of a material with a lower surface resistivity without incurring a penalty in the power consumed. The electrically resistive skins are typically processed a resistivity in the range of 10^6 to 10^9 ohm-cm.

Fig. 10 is a perspective view of a wafer 500 formed in accordance with Method (3). In one embodiment, wafer 500 has a thickness of approximately 100 μm .

Fig. 11 depicts a spacer 510 formed from wafer 500. Electrically resistive skins 502 and 503 provide a gradual transition from a relatively low surface resistivity at outside surfaces 504 and 505 to a relatively high bulk resistivity at core 501. Face metallization strips 516 and 517 are formed on outside surface 504, and face metallization strips 519 and 520 are formed on outside surface 505 of spacer 510. Edge metallization strips 524 and 525 are formed on edge surfaces 526 and 527, respectively. Metallization strips 516-517, 519-520 and 524-525 are formed in a manner similar to that previously described in connection with Method (1).

In a variation of Method (3), wafer 500 is slit into strips before the initial firing step. When the strips are fired in the reducing atmosphere, the transition metal oxide at all of the exterior surfaces (including outside surfaces 504 and 505 and edge surfaces 526 and 527) becomes electrically resistive.

In another variation of Method (3), B_2O_3 is included in the ceramic composition to lower the firing temperature and the resistivity without raising the secondary electron emission of the resulting spacer.

A spacer fabricated in accordance with Method (3) advantageously has a high bulk resistivity and a low secondary emission coefficient. Such a spacer therefore results in reduced power loss and reduced voltage variations proximate the spacer during operation of the flat panel display.

Turning now to Method (4), a wafer 600 is formed by placing an electrically resistive coating onto a solid electrically insulating core, and firing the resulting structure. Fig. 12 depicts a wafer 600 formed in accordance with Method (4). Solid, electrically insulating core 601 can be fabricated by casting or compacting 100% alumina ceramic into a tape having a thickness of 100 μm . The tape is cut into wafers (or strips) and fired at a temperature between 1500 and 1700°C for approximately two hours.

Electrically resistive coatings 602 and 603 are applied to core 601 while core 601 is in a large wafer format. Core 601 and resistive coatings 602-602 are fired and then cut into strips to make spacers.

Electrically resistive coatings 602 and 603 are applied to core 601 using any method which can be used to apply paint or dye to a surface. These methods include screen printing, spraying, roll coating, doctor blading or applying a decal. Some of these methods are described below.

In screen printing, the resistive material is applied as a paste or ink which is formed by placing the resistive material in an organic suspension. The suspension is forced through a mesh (usually stainless steel) in a manner very similar to that used to make decorative patterns on T-shirts or to print posters. The paste is placed on top of the screen and a squeegee blade rubs a thin coat of paste through the screen onto the underlying core 601. By proper choice of the consistency of the paste, the opening and thickness of

the mesh and the speed and softness of the squeegee, a precisely controlled layer of the paste is transferred to core 601.

5 Alternatively the resistive material may be dispersed as a thinner liquid and sprayed onto the surface of core 601. This process is similar to paint spraying.

10 In roll coating, a thin layer of the resistive material in an organic suspension is squeezed onto the surface of core 601 by passing the substrate under specially grooved rubber rollers. By choosing the configuration of the grooves and compounding the organic suspension to suit this configuration, thin resistive coatings 602 and 603 placed on core 601 at
15 very high speeds.

Precise coating thicknesses can also be applied by doctor blading. In doctor blading, a pool of the resistive material in an organic suspension is trapped behind a blade positioned above core 601. By moving
20 core 601 relative to the blade and the pool at a constant speed, a constant and controlled thickness of the material is dragged under the blade and onto the surface.

The resistive material can also be dispersed in an
25 organic material to form a tape using a method similar to the tape preparation methods previously described. This tape is cut to match the size of core 601, and pressed onto core 601. The plastic component of core 601 is chosen to provide adhesion or a separate
30 adhesive layer may be applied.

Acceptable resistive materials include, but are not limited to, the various electrically resistive ceramic compositions previously described. Core 601 and electrically resistive coatings 602 and 603 are
35 fired in accordance with the parameters previously set forth in connection with Method (1). The fired wafer

600 is processed in the same manner as previously described in connection with Method (1).

Fig. 13 shows a spacer 610 formed from wafer 600. Spacer 610 includes electrically insulating core 601 and electrically resistive coatings 602 and 603. Face metallization strips 615 and 616 are formed on outside surface 617 of spacer 610, and face metallization strips 619 and 620 are formed on outside surface 621 of spacer 610. Edge metallization strips 624 and 625 are formed on edge surfaces 626 and 627 of spacer 610.

In a variation of Method (4), the resistive coatings 602 and 603 are applied to insulating core 601 before the insulating core 601 is fired. Again, acceptable resistive coatings include, but are not limited to, the previously described combinations of alumina and transition metal oxides. The electrically resistive coatings are typically applied by screen printing, spray painting, roll coating, doctor blading or applying a decal. This variation of Method (4) may require an additional reduction step if the diffusion of the resistive coatings 602-603 into core 601 produce layers which are lower in conductivity than desired. In general, the greater the extent of the diffusion, the lower the conductivity of coatings 602-603. If the lattice chosen allows non-reconstructive reformation of the crystal (e.g., filling of oxygen vacancies), the reduction step provides a thin conductive layer on the surface of coatings 602-603 in a manner similar to that previously described in connection with Method (3).

The remaining steps of this variation of Method (4) are similar to the steps previously described in connection with Method (1).

In another variation of Method (4), resistive coatings 602 and 603 are formed from conductive glazes developed for suppressing electrical breakdown in high voltage insulators. These glazes exhibit the desired

electrical resistivity and can be processed at reasonably low temperatures. Transition metals, such as iron, chromium, or titanium, can also be dissolved in these glazes to form acceptable resistive coatings.

5 There are a number of commercial compositions used for this purpose. Most contain dissolved iron, titanium and/or chromium in the form of oxides.

Although Methods (1) through (4) are described in connection with alumina ceramic cores, it is possible

10 to use other ceramic compositions, such as mullites, cordierites, barium borosilicates, iron silicates, filled glasses, and zero shrink tolerance (ZST) materials. ZST materials obtain their unique properties by balancing the behavior of glass and

15 ceramic filler components. A transition metal oxide can be admixed into the glass component without drastically altering the properties of the ZST material. Because the glass forms a continuous matrix throughout the structure of the ZST material, making

20 the glass phase a controlled conductor is sufficient to control the electrical resistivity of the spacer.

Although certain of the previously described spacers have been described as having both face and edge metallization strips, these spacers may

25 alternatively include only edge metallization strips or only face metallization strips. Moreover, each of these spacers may also include potential adjustment electrodes as described in connection with Method (1).

Various embodiments of the invention have been

30 described. The descriptions are intended to be illustrative, not limiting. For example, the length of the spacers can be varied such that the spacers resemble "posts" or "walls." Thus, it will be apparent to one skilled in the art that modifications may be

35 made to the invention as described without departing from the scope of the claims set out below.

WE CLAIM:

1. A spacer comprising:
a ceramic; and
transition metal oxide dispersed in the
5 ceramic.
2. The spacer of Claim 1, wherein the ceramic is
alumina.
- 10 3. The spacer of Claim 1, wherein the transition
metal oxide is titania, chromia, iron oxide or vanadium
oxide.
4. The spacer of Claim 1, wherein the transition
15 metal oxide consists of titania and chromia.
5. The spacer of Claim 4, wherein the ceramic
contains 0.25 to 8 % titania.
- 20 6. The spacer of Claim 4, wherein the spacer
comprises approximately 2 percent titanium, 34 percent
alumina and 64 percent chromia.
7. A flat panel display comprising:
25 a faceplate structure having a faceplate and
a light emitting structure located along an
interior surface of the faceplate;
a backplate structure having a backplate and
an electron emitting structure located along an
30 interior surface of the backplate; and
a spacer which extends between the light
emitting structure and the electron emitting
structure, wherein the spacer comprises a ceramic
and transition metal oxide dispersed in the
35 ceramic.

8. The flat panel display of Claim 7, wherein the spacer further comprises:

a first face metallization strip situated along an outside surface of the spacer adjacent to the light emitting structure; and

a second face metallization strip situated along the outside surface of the spacer adjacent to the electron emitting structure.

9. The flat panel display of Claim 8, wherein the first face metallization strip electrically contacts the light emitting structure, and the second face metallization strip electrically contacts the electron emitting structure.

10. The flat panel display of Claim 9, wherein the electron emitting structure comprises one or more focusing ridges, and the second face metallization strip electrically contacts the focusing ridges.

11. The flat panel display of Claim 7, further comprising:

a first face metallization strip situated along an outside surface of the spacer; and

electrically conductive frit formed along an outer edge of the faceplate structure, wherein the first face metallization strip electrically contacts the frit.

12. The flat panel display of Claim 10, wherein the electrically conductive frit is screen-printed on the faceplate structure.

13. The flat panel display of Claim 8, wherein the spacer has a first edge surface positioned adjacent to the light emitting structure and a second edge

surface positioned adjacent to the electron emitting structure, the flat panel display further comprising:

5 a first edge metallization strip situated over the first edge surface and contacting the first face metallization strip and the light emitting structure; and
10 a second edge metallization strip situated over the second edge surface and contacting the second face metallization strip and the electron emitting structure.

14. The flat panel display of Claim 8, further comprising:

15 a plurality of potential adjustment electrodes provided over the outside surface of the spacer at intervals; and
a power supply circuit connected to the first and second face metallization strips, wherein the power supply circuit controls the voltage
20 distribution between the light emitting structure and the electron emitting structure.

15. The flat panel display of Claim 14, wherein the power supply circuit is connected to the potential
25 adjustment electrodes.

16. The flat panel display of Claim 14, wherein each of the potential adjustment electrodes is located on the same surface of the spacer.
30

17. The flat panel display of Claim 16, wherein the first and second face metallization strips are located on the same surface of the spacer as the potential adjustment electrodes.
35

18. The flat panel display of Claim 7, wherein the spacer has a first edge surface positioned adjacent to the light emitting structure and a second edge surface positioned adjacent to the electron emitting structure, the flat panel display further comprising:

5 a first edge metallization strip situated along the first edge surface and electrically contacting the light emitting structure; and
a second edge metallization strip situated
10 along the second edge surface and electrically contacting the electron emitting structure.

19. A spacer comprising:
an electrically insulating ceramic core
15 having an outside surface; and
an electrically resistive skin situated over the outside surface, the electrically resistive skin comprising a ceramic and transition metal oxide dispersed in the ceramic.

20
20. The spacer of Claim 19, wherein the insulating ceramic core comprises alumina.

21. The spacer of Claim 19, wherein the ceramic
25 is alumina and the transition metal oxide is titania, chromia or iron oxide.

22. The spacer of Claim 19, wherein the ceramic
is alumina and the transition metal oxide comprises
30 chromia and titania.

23. The spacer of Claim 19, wherein the insulating ceramic core comprises alumina containing transition metal oxide, wherein the transition metal
35 oxide is present in the higher oxide states.

24. The spacer of Claim 19, wherein the transition metal oxide is present in the lower oxide states.

5 25. The spacer of Claim 19, wherein the electrically resistive skin comprises a thin wafer laminated onto the outside surface.

26. A flat panel display comprising:
10 a faceplate structure having a faceplate and a light emitting structure located along an interior surface of the faceplate;
 a backplate structure having a backplate and an electron emitting structure located along an
15 interior surface of the backplate;
 a spacer which extends between the light emitting structure and the electron emitting structure, wherein the spacer comprises an
20 electrically insulating ceramic core and an electrically resistive skin situated over an outside surface of the spacer, the electrically resistive skin comprising a ceramic and transition metal oxide dispersed in the ceramic.

25 27. The flat panel display of Claim 26, wherein the spacer further comprises:
 a first face metallization strip situated along an outside surface of the spacer adjacent to the light emitting structure; and
30 a second face metallization strip situated along the outside surface of the spacer adjacent to the electron emitting structure.

28. The flat panel display of Claim 27, wherein
35 the first face metallization strip electrically contacts the light emitting structure, and the second

face metallization strip electrically contacts the electron emitting structure.

29. The flat panel display of Claim 28, wherein
5 the electron emitting structure comprises one or more focusing ridges, and the second face metallization strip electrically contacts the focusing ridges.

30. The flat panel display of Claim 27, further
10 comprising electrically conductive frit formed along an outer edge of the faceplate structure, wherein the first face metallization strip electrically contacts the frit.

31. The flat panel display of Claim 27, wherein
15 the spacer has a first edge surface positioned adjacent to the light emitting structure and a second edge surface positioned adjacent to the electron emitting structure, wherein the spacer further comprises:
20 a first edge metallization strip situated over the first edge surface and electrically contacting the first face metallization strip and the light emitting structure; and
a second edge metallization strip situated
25 over the second edge surface and electrically contacting the second face metallization strip and the electron emitting structure.

32. The flat panel display of Claim 27, further
30 comprising:
a plurality of potential adjustment electrodes provided over the outside surface of the spacer at intervals; and
a power supply circuit connected to the first
35 and second face metallization strips, wherein the power supply circuit controls the voltage

distribution between the light emitting structure and the electron emitting structure.

33. The flat panel display of Claim 32, wherein
5 the power supply circuit is connected to the potential adjustment electrodes.

34. The flat panel display of Claim 32, wherein
10 the first and second face metallization strips and the potential adjustment electrodes are located on the same surface of the spacer.

35. The flat panel display of Claim 26, wherein
15 the spacer has a first edge surface positioned adjacent to the light emitting structure and a second edge surface positioned adjacent to the electron emitting structure, the flat panel display further comprising:
a first edge metallization strip situated
20 along the first edge surface and electrically contacting the light emitting structure; and
a second edge metallization strip situated
along the second edge surface and electrically contacting the electron emitting structure.

25 36. A method of fabricating spacers comprising the steps of:

forming a wafer from a ceramic composition comprising electrically insulating ceramic and transition metal oxide;
30 firing the wafer until the wafer exhibits a desired electrical resistivity;
forming face metallization strips over opposing outside surfaces of the wafer;
firing the wafer and face metallization
35 strips; and

cutting the wafer along the face
metallization strips, thereby forming the spacers.

37. The method of Claim 36, wherein the step of
5 firing the wafer until the wafer exhibits a desired
electrical resistivity is performed in a reducing
atmosphere.

38. The method of Claim 36, wherein the step of
10 forming the face metallization strips comprises
evaporating metal onto the wafer.

39. The method of Claim 38, wherein the metal
comprises aluminum, chromium or nickel.
15

40. The method of Claim 36, further comprising
the step of forming edge metallization strips over edge
surfaces of the spacers.

20 41. The method of Claim 36, wherein the step of
forming face metallization strips further comprises
forming potential adjustment electrodes over at least
one of the opposing outside surfaces of the wafer.

25 42. The method of Claim 36, wherein the cutting
step is performed prior to the wafer firing step.

43. A method of fabricating spacers comprising
the steps of:
30 forming a first wafer from electrically
insulating ceramic;
forming a second wafer from a ceramic
composition comprising an electrically insulating
ceramic containing transition metal oxide
35 dispersed in the ceramic; and

attaching the first and second wafers to form a laminated wafer.

5 44. The method of Claim 43, further comprising the steps of:

 firing the laminated wafer until the second
 wafer exhibits a desired electrical resistivity;
 forming face metallization strips along
 outside surfaces of the laminated wafer; and
10 cutting the laminated wafer along the face
 metallization strips, thereby forming the spacers.

 45. The method of Claim 43, wherein the
 insulating ceramic comprises alumina.
15

 46. The method of Claim 43, wherein the laminated
 wafer firing step comprises firing the laminated wafer
 in a reducing atmosphere.

20 47. The method of Claim 44, wherein the step of
 forming the face metallization strips further comprises
 evaporating metal onto the outside surfaces of the
 laminated wafer.

25 48. The method of Claim 47, wherein the metal
 comprises aluminum, chromium or nickel.

 49. The method of Claim 43, further comprising
 the step of forming edge metallization strips over edge
30 surfaces of the spacers.

 50. The method of Claim 43, further comprising
 the step of forming face metallization strips and
 potential adjustment electrodes on the laminated wafer.
35

51. The method of Claim 50, wherein the face metallization strips and potential adjustment electrodes are fabricated on only one side of the laminated wafer.

5

52. A method of fabricating spacers comprising the steps of:

forming a wafer from an electrically insulating ceramic composition comprising electrically insulating ceramic and transition metal oxide, wherein the transition metal oxide is present in the higher oxide states;

firing the wafer in a reducing atmosphere such that the coordination of the transition metal oxide is altered, thereby causing the transition metal oxide to be present in the lower oxide states at the outer surfaces of the wafer, thereby also causing the outer surfaces of the wafer to become electrically resistive.

20

53. The method of Claim 52, further comprising the steps of:

forming face metallization strips over the outside surfaces of the wafer; and cutting the wafer along the face metallization strips, thereby forming the spacers.

25

54. The method of claim 52, wherein the ceramic composition comprises alumina and Cr_2O_3 .

30

55. The method of claim 54, wherein the ceramic composition further comprises B_2O_3 .

56. The method of Claim 52, wherein the step of forming the face metallization strips comprises evaporating metal onto the wafer.

35

57. The method of Claim 56, wherein the metal comprises aluminum, chromium or nickel.

58. The method of Claim 52, further comprising
5 the step of forming edge metallization strips over edge surfaces of the spacers.

59. The method of Claim 52, wherein the step of
forming face metallization strips further comprises
10 forming potential adjustment electrodes over at least one of the outer surfaces of the wafer.

60. The method of Claim 52, wherein the step of
forming face metallization strips further comprises
15 forming potential adjustment electrodes over only one of the outer surfaces of the wafer.

61. A method of fabricating spacers comprising
the steps of:
20 forming a core wafer from electrically insulating ceramic; and
applying an electrically resistive coating
onto a surface of the core wafer, the resistive
coating comprising an electrically insulating
25 ceramic and transition metal oxide dispersed in the ceramic.

62. The method of Claim 61, further comprising
the steps of:
30 firing the core wafer and the resistive coating;
forming face metallization strips along
outside surfaces of the resistive coating; and
cutting the resulting structure along the
35 face metallization strips, thereby forming the spacers.

63. The method of Claim 61, further comprising the step of firing the core wafer prior to applying the resistive coating.

5 64. The method of Claim 61, wherein the applying step comprises screen printing, spraying, roll coating or doctor blading the resistive coating over the core wafer, or applying a decal containing the resistive coating to the core wafer.

10 65. The method of Claim 61, wherein the insulating ceramic is alumina.

15 66. The method of Claim 61, wherein the resistive coating comprises alumina containing chromia, titania, iron oxide or vanadium oxide.

20 67. The method of Claim 61, wherein the step of forming the face metallization strips comprises evaporating metal onto the resistive coating.

 68. The method of Claim 67, wherein the metal comprises aluminum, chromium or nickel.

25 69. The method of Claim 61, further comprising the step of forming edge metallization strips over edge surfaces of the spacers.

30 70. The method of Claim 61, wherein the step of forming face metallization strips further comprises forming potential adjustment electrodes over at least one of the outside surfaces of the resistive coating.

35 71. The method of Claim 61, wherein the step of forming face metallization strips further comprises

forming potential adjustment electrodes over only one of the outside surfaces of the resistive coating.

72. A method of fabricating spacers comprising
5 the steps of:

forming a wafer from a ceramic composition
comprising electrically insulating ceramic and
transition metal oxide dispersed in the ceramic;
forming a face metallization layer over the
10 wafer;
attaching the wafer to a substrate;
patterning the face metallization layer into
a plurality of face metallization strips;
forming a protective layer over the face
15 metallization strips and wafer;
cutting the wafer into spacer strips;
forming an edge metallization layer over the
spacer strips;
removing the protective layer; and
20 detaching the spacer strips from the
substrate.

73. A spacer comprising:
electrically insulating glass;
25 transition metal oxide dissolved in the
glass, wherein the transition metal oxide causes
the spacer to exhibit a desired electrical
resistivity; and
a filler interspersed within the glass,
30 wherein the filler causes the spacer to exhibit a
desired secondary electron emission.

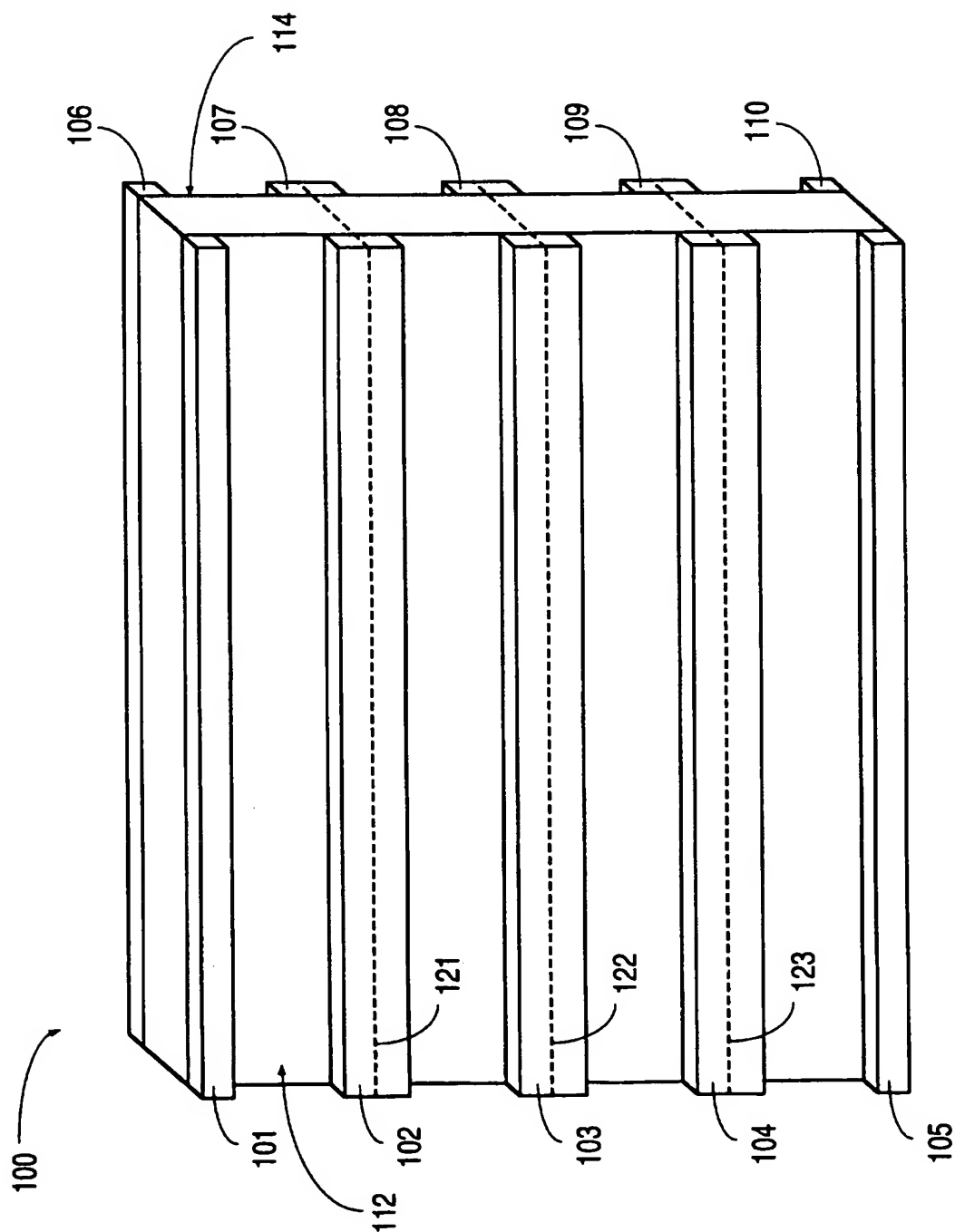


FIG. 1

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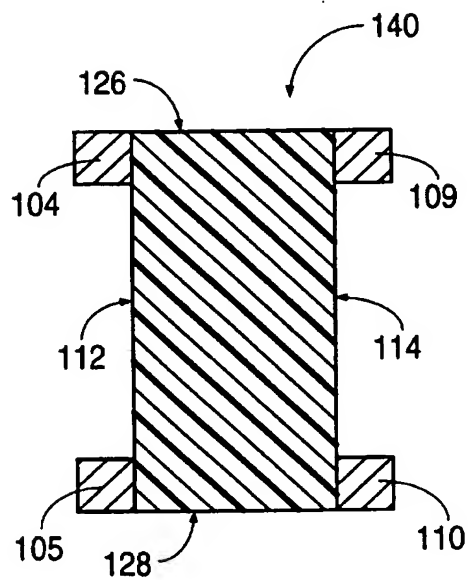


FIG. 2

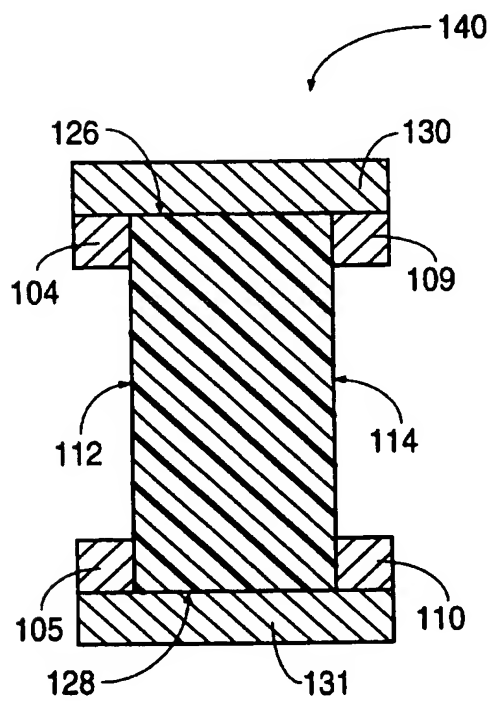


FIG. 3

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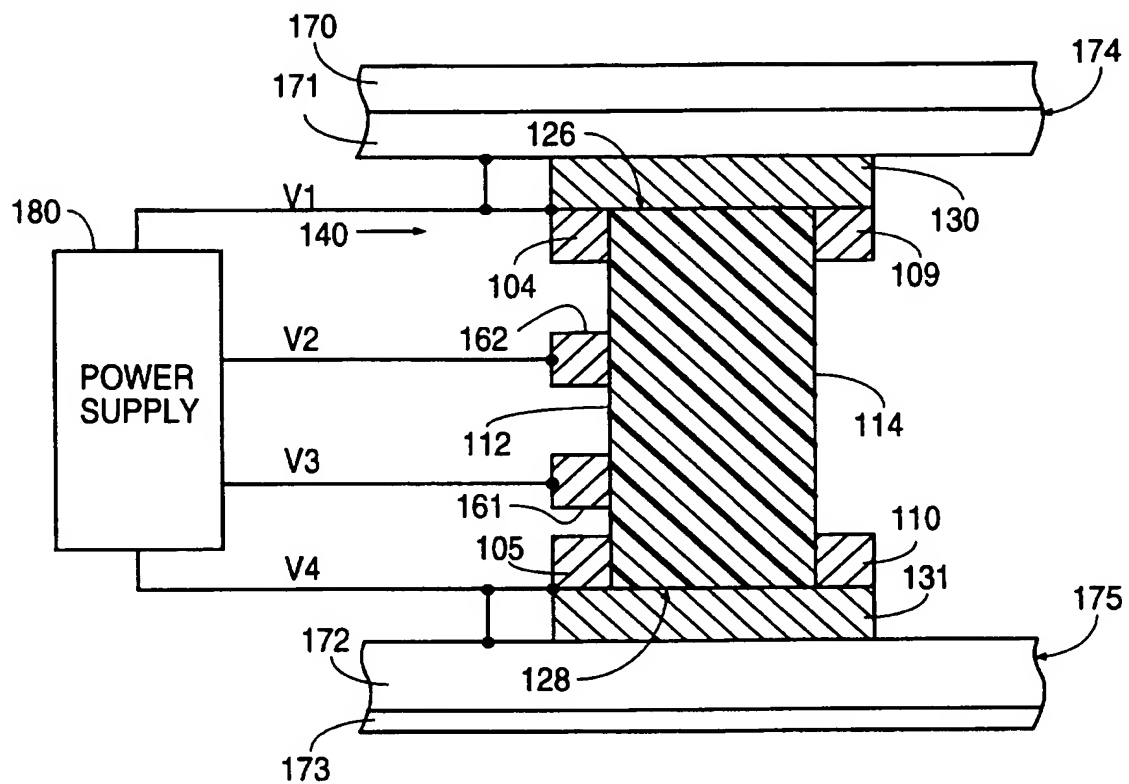


FIG. 4

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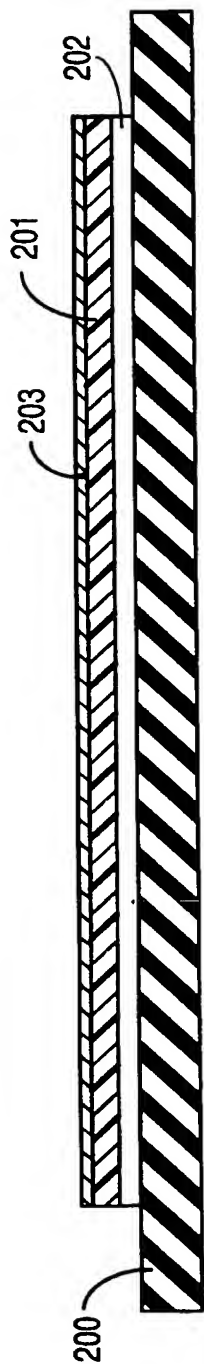


FIG. 5a

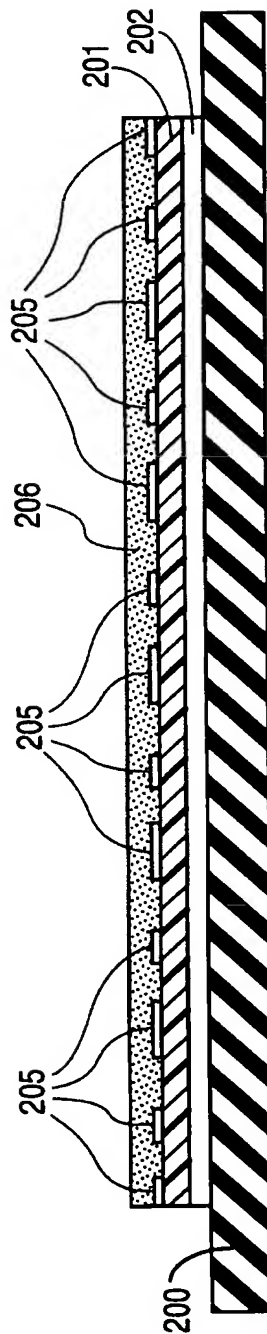


FIG. 5b

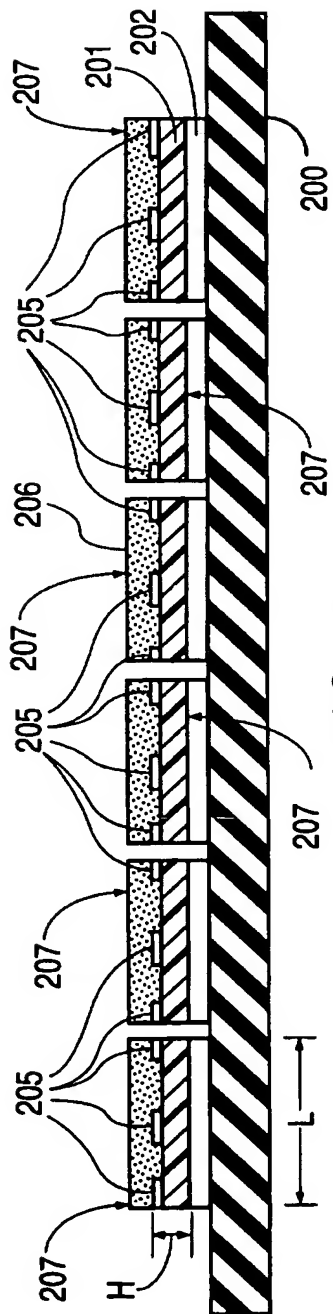


FIG. 5c

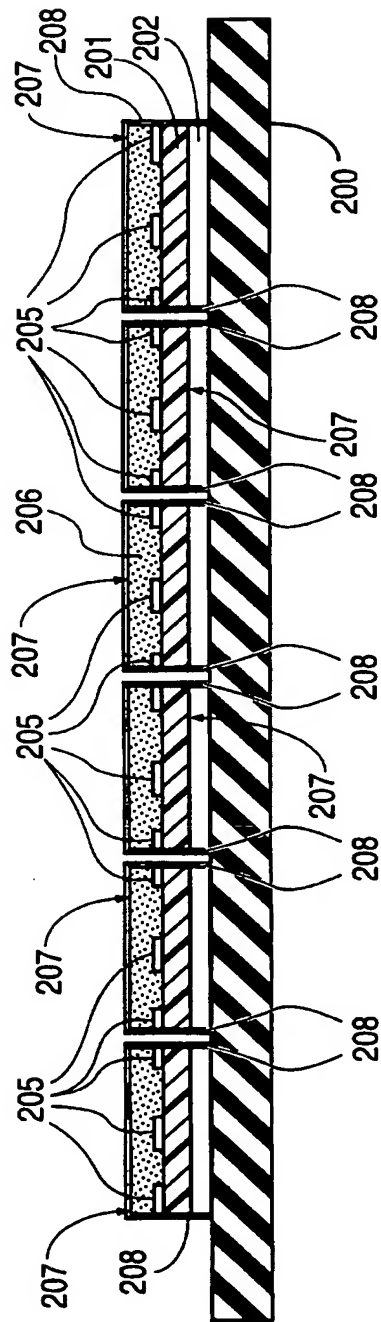


FIG. 5d

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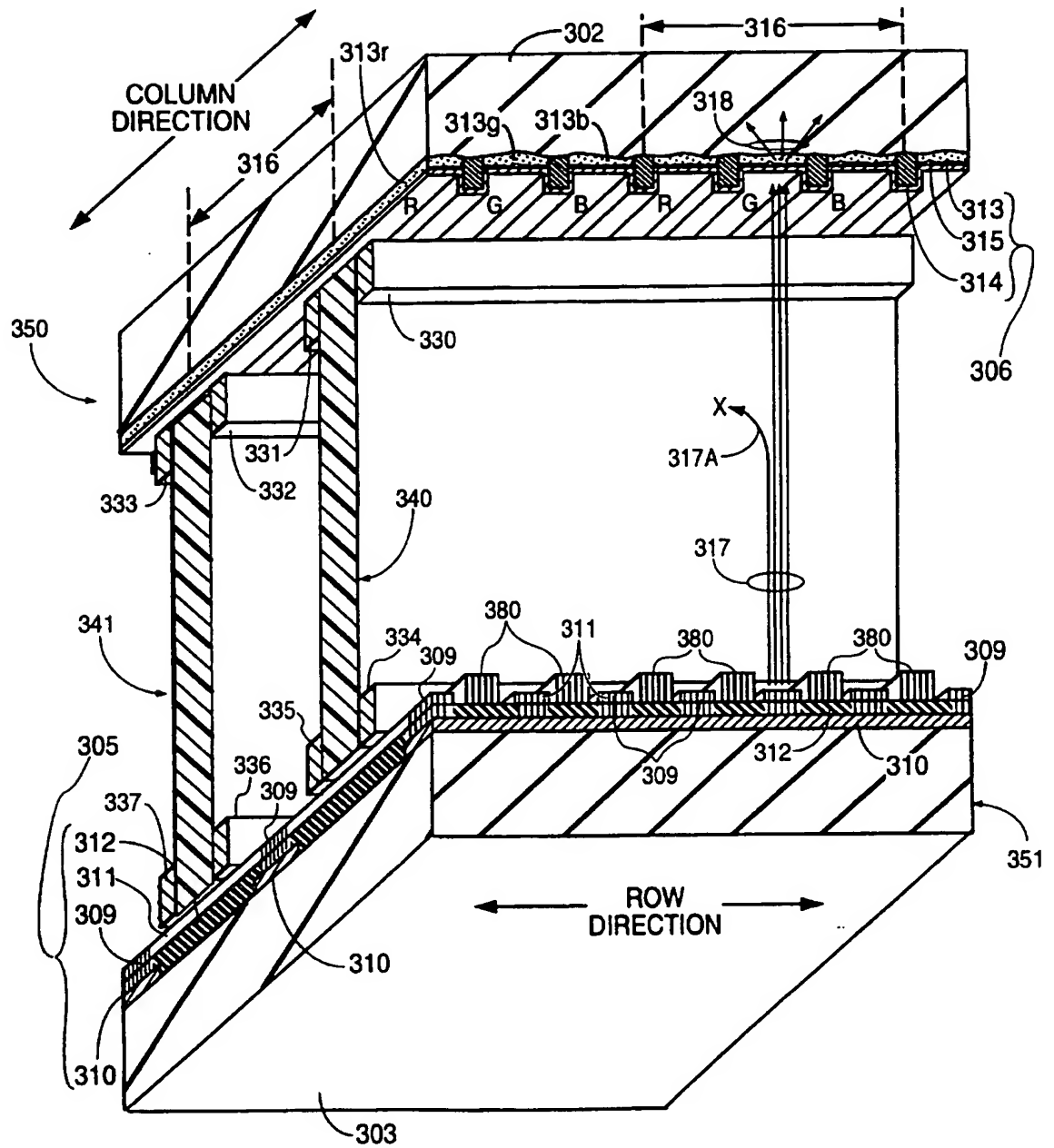


FIG. 6

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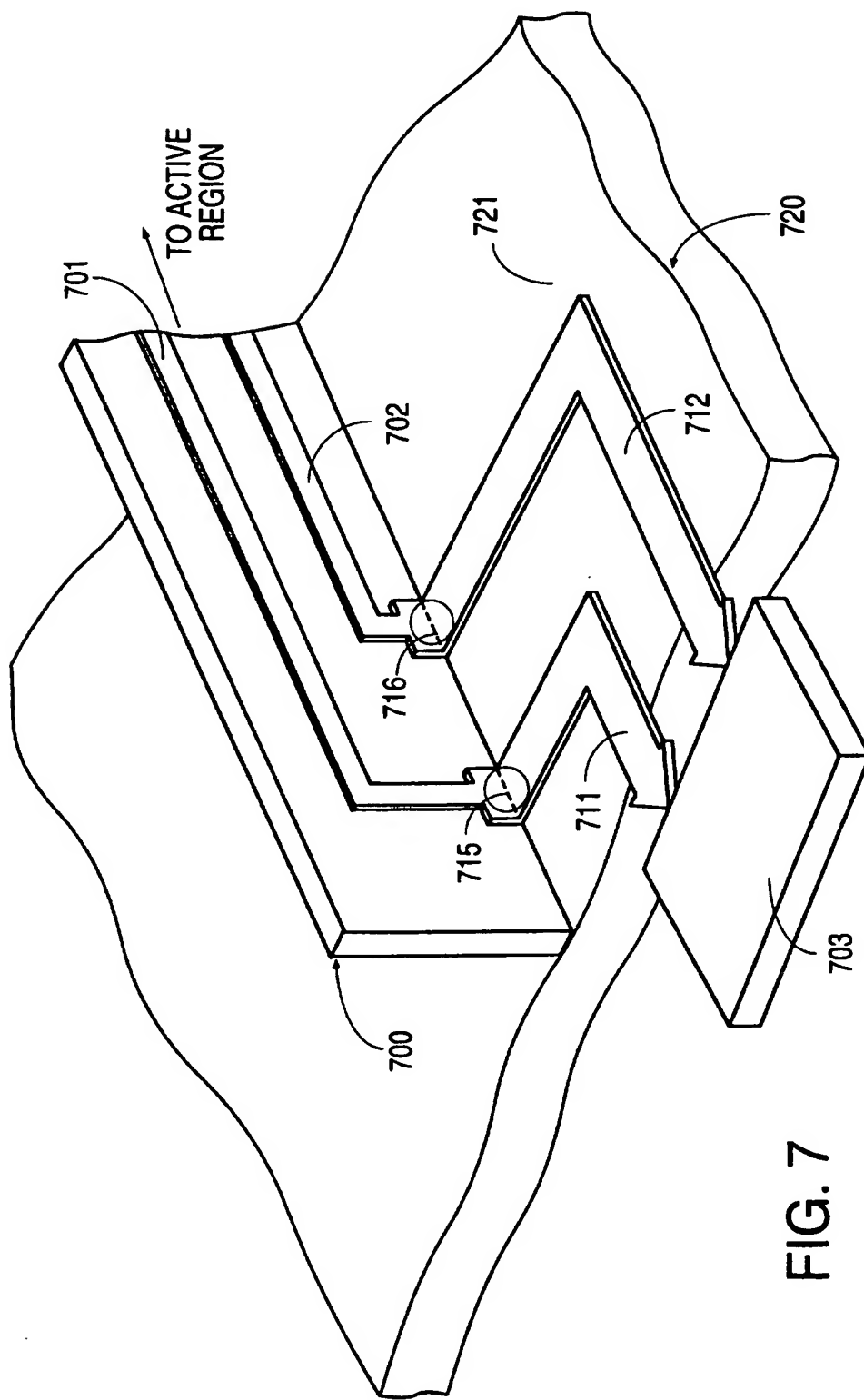


FIG. 7

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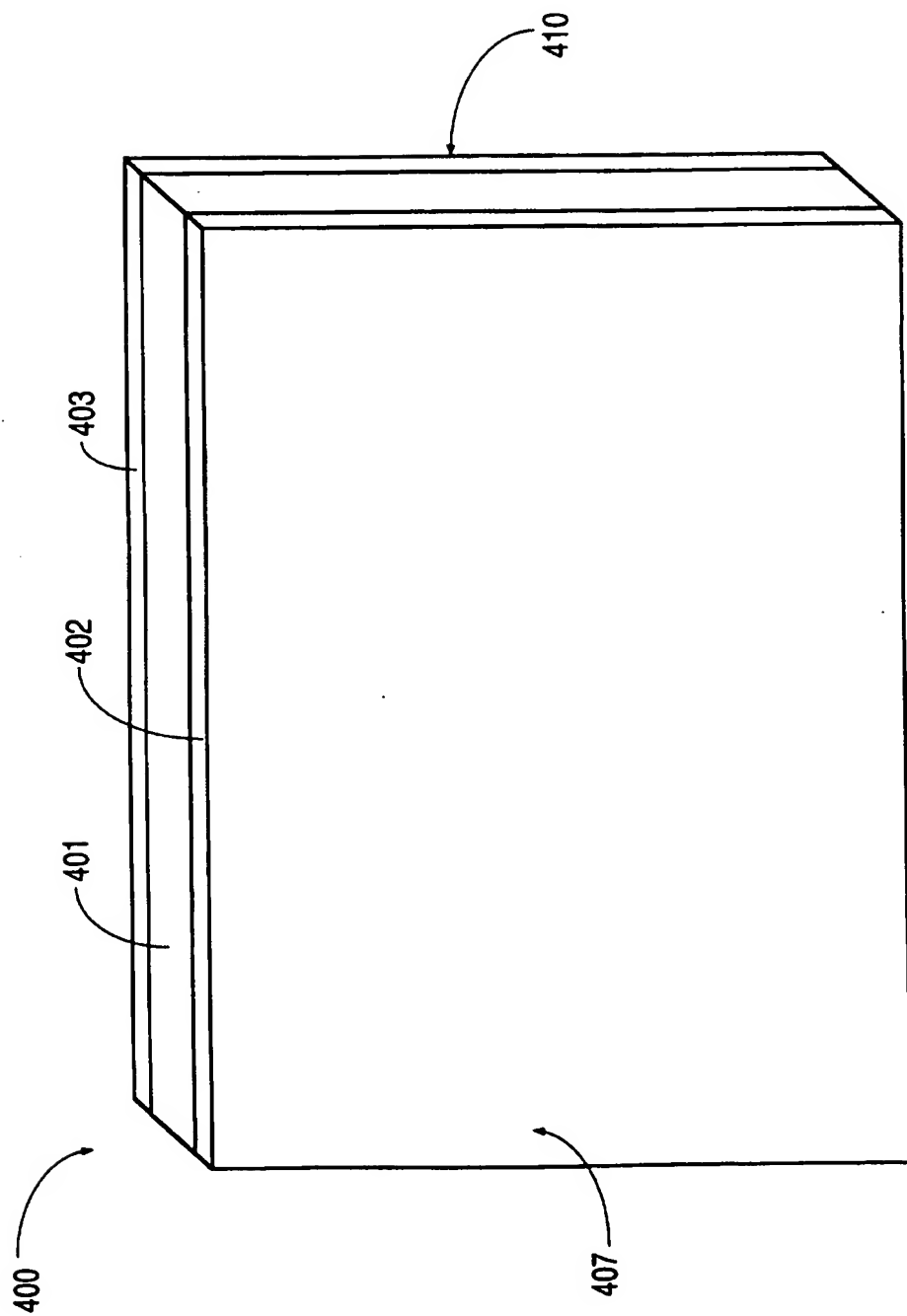


FIG. 8

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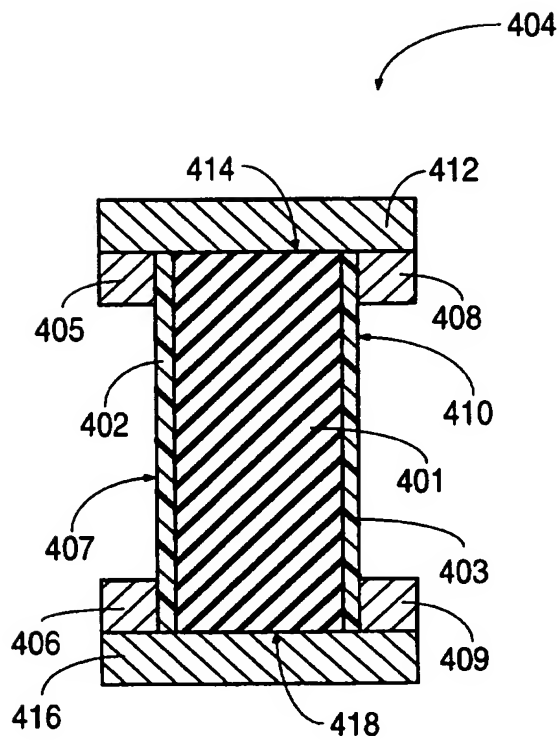


FIG. 9

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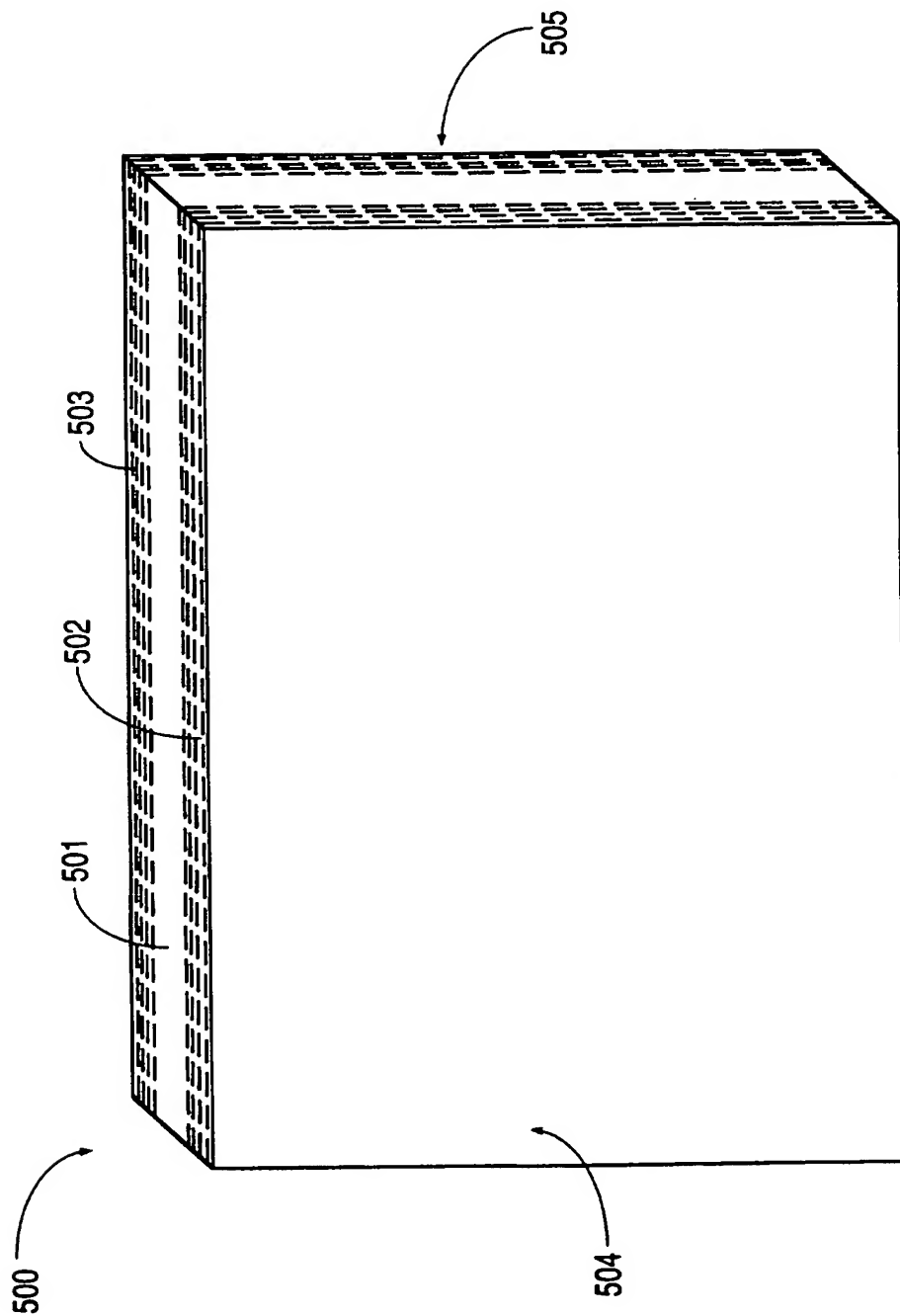


FIG. 10

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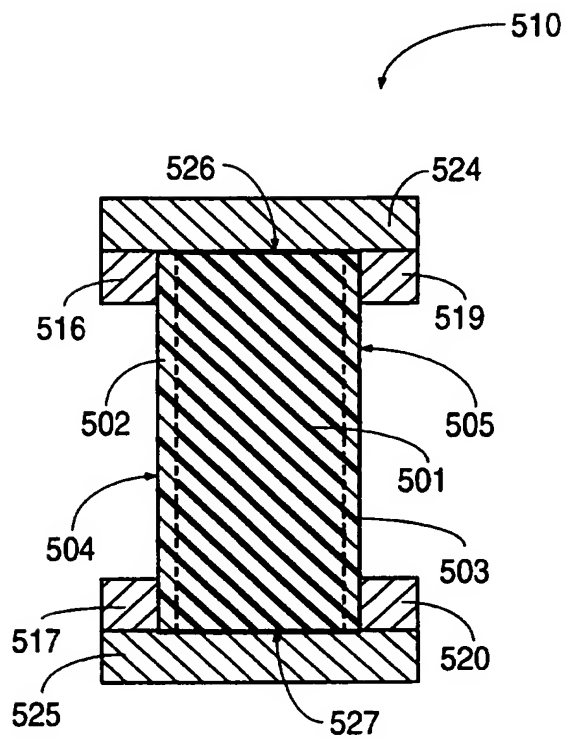


FIG. 11

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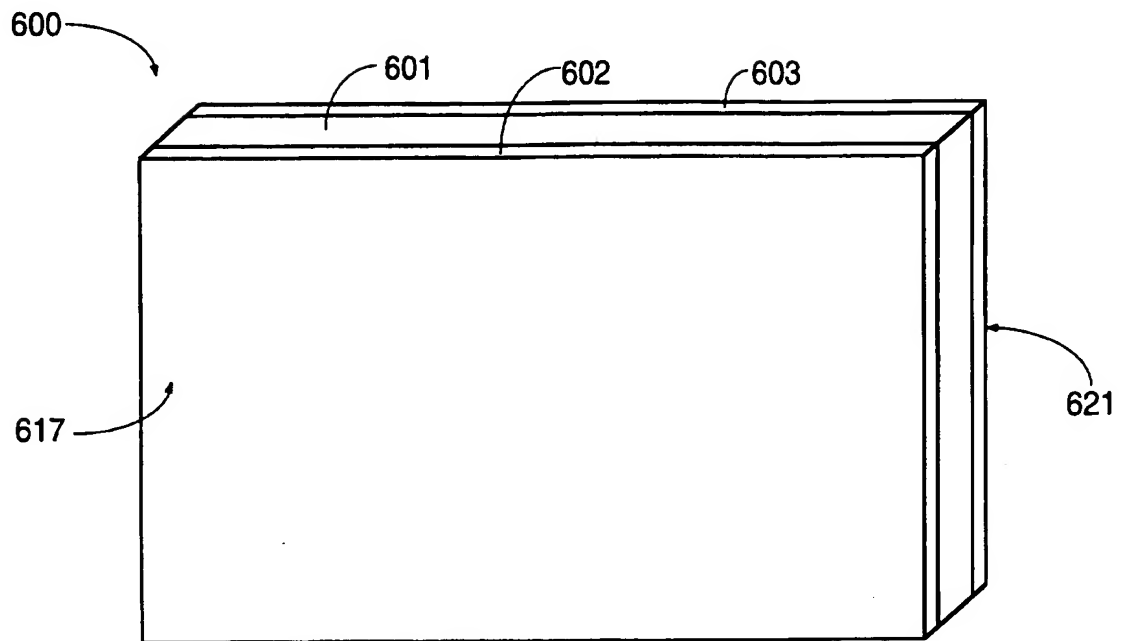


FIG. 12

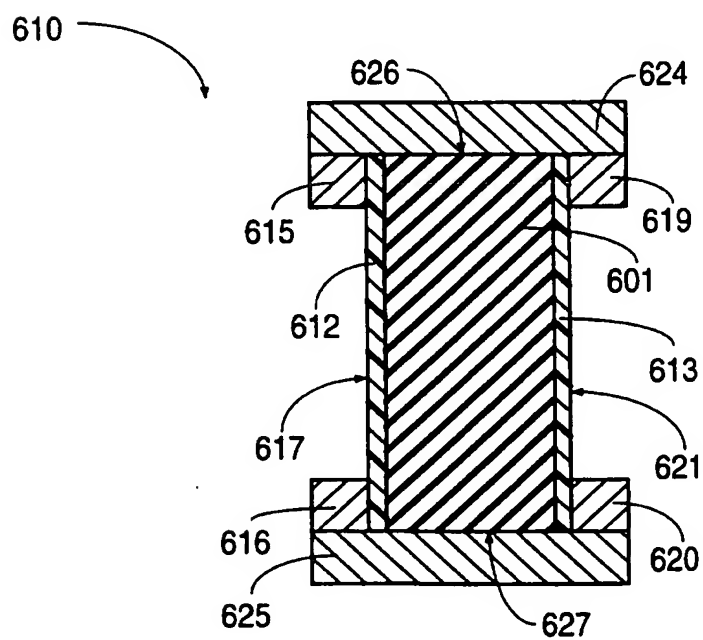


FIG. 13

INTERNATIONAL SEARCH REPORT

International Application No

PC 1/US 96/03640

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01J31/12 H01J9/18 H01J29/82

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H01J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO,A,94 18694 (SILICON VIDEO CORP) 18 August 1994 cited in the application see claims 1,3 see page 39, line 15 - line 27 see page 44, line 19 - page 46, line 14	1,3-10, 73
Y	---	2
Y	US,A,4 021 219 (STOCKDALE GEORGE FAIRBANK ET AL) 3 May 1977 see column 6, line 53 - line 59 ---	2
X	PATENT ABSTRACTS OF JAPAN vol. 008, no. 047 (M-280), 2 March 1984 & JP,A,58 202711 (MITSUBISHI KINZOKU KK), 26 November 1983, see abstract ---	1
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☒ Further documents are listed in the continuation of box C.☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

23 July 1996

Date of mailing of the international search report

- 2. 08. 96

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 96/03640

C(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
3 P,X	EP,A,0 690 476 (HAMAMATSU PHOTONICS KK) 3 January 1996 see column 1, line 21 - line 23 see column 1, line 53 - line 56 ---	1,2
6 A	EP,A,0 405 262 (MATSUSHITA ELECTRIC IND CO LTD) 2 January 1991 see column 9, line 29 - column 10, line 1 ---	1,7,19, 26,36, 43,52, 61,72,73
1 A	EP,A,0 580 244 (PHILIPS ELECTRONICS NV) 26 January 1994 cited in the application see column 4, line 46 - line 54 see column 9, line 11 - line 41 see column 12, line 25 - line 40 -----	1,7,19, 26,36, 43,52, 61,72,73

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 96/03640

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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US-A-4021219	03-05-77	NONE	
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EP-A-0405262	02-01-91	JP-A- 3022328 JP-A- 3049135 JP-B- 7099679 DE-D- 69009307 DE-T- 69009307 US-A- 5083058	30-01-91 01-03-91 25-10-95 07-07-94 26-01-95 21-01-92
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